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**Algorithms
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*Research and
development of logic
synthesis and
verification have*

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*matured considerably
over the past two
decades. Many
commercial products
are available, and
they have been critical
in harnessing
advances in
fabrication
technology to produce
today's plethora of
electronic
components. While*

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this maturity is assuring, the advances in fabrication continue to seemingly present unwieldy challenges. Logic Synthesis and Verification provides a state-of-the-art view of logic synthesis and verification. It consists of fifteen chapters, each

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focusing on a distinct aspect. Each chapter presents key developments, outlines future challenges, and lists essential references. Two unique features of this book are technical strength and comprehensiveness. The book chapters are written by twenty-

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*eight recognized
leaders in the field
and reviewed by
equally qualified
experts. The topics
collectively span the
field. Logic Synthesis
and Verification fills
a current gap in the
existing CAD
literature. Each
chapter contains
essential information*

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to study a topic at a great depth, and to understand further developments in the field. The book is intended for seniors, graduate students, researchers, and developers of related Computer-Aided Design (CAD) tools. From the foreword:

"The commercial

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*success of logic
synthesis and
verification is due in
large part to the ideas
of many of the
authors of this book.
Their innovative work
contributed to design
automation tools that
permanently changed
the course of
electronic design."* by
Aart J. de Geus,

***Chairman and CEO,
Synopsys, Inc.***

***Design and
optimization of
integrated circuits are
essential to the
creation of new
semiconductor chips,
and physical
optimizations are
becoming more
prominent as a result
of semiconductor***

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scaling. Modern chip design has become so complex that it is largely performed by specialized software, which is frequently updated to address advances in semiconductor technologies and increased problem complexities. A user of such software

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needs a high-level understanding of the underlying mathematical models and algorithms. On the other hand, a developer of such software must have a keen understanding of computer science aspects, including algorithmic performance

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*bottlenecks and how
various algorithms
operate and interact.*

*"VLSI Physical
Design: From Graph
Partitioning to
Timing Closure"
introduces and
compares algorithms
that are used during
the physical design
phase of integrated-
circuit design,*

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wherein a geometric chip layout is produced starting from an abstract circuit design. The emphasis is on essential and fundamental techniques, ranging from hypergraph partitioning and circuit placement to timing closure.

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*The first of two
volumes in the
Electronic Design
Automation for
Integrated Circuits
Handbook, Second
Edition, Electronic
Design Automation
for IC System Design,
Verification, and
Testing thoroughly
examines system-level
design,*

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*microarchitectural
design, logic
verification, and
testing. Chapters
contributed by leading
experts authoritatively
discuss processor
modeling and design
tools, using
performance metrics
to select
microprocessor cores
for integrated circuit*

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*(IC) designs, design
and verification
languages, digital
simulation, hardware
acceleration and
emulation, and much
more. New to This
Edition: Major
updates appearing in
the initial phases of
the design flow,
where the level of
abstraction keeps*

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*rising to support more
functionality with
lower non-recurring
engineering (NRE)
costs Significant
revisions reflected in
the final phases of
the design flow,
where the complexity
due to smaller and
smaller geometries is
compounded by the
slow progress of*

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*shorter wavelength
lithography New
coverage of cutting-
edge applications and
approaches realized
in the decade since
publication of the
previous
edition—these are
illustrated by new
chapters on high-level
synthesis, system-on-
chip (SoC) block-*

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*based design, and
back-annotating
system-level models
Offering improved
depth and modernity,
Electronic Design
Automation for IC
System Design,
Verification, and
Testing provides a
valuable, state-of-the-
art reference for
electronic design*

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automation (EDA)
students, researchers,
and professionals.

*This book provides
readers with an up-to-
date account of the
use of machine
learning frameworks,
methodologies,
algorithms and
techniques in the
context of computer-
aided design (CAD)*

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*for very-large-scale
integrated circuits
(VLSI). Coverage
includes the various
machine learning
methods used in
lithography, physical
design, yield
prediction, post-
silicon performance
analysis, reliability
and failure analysis,
power and thermal*

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analysis, analog design, logic synthesis, verification, and neuromorphic design. Provides up-to-date information on machine learning in VLSI CAD for device modeling, layout verifications, yield prediction, post-silicon validation, and reliability; Discusses

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the use of machine learning techniques in the context of analog and digital synthesis; Demonstrates how to formulate VLSI CAD objectives as machine learning problems and provides a comprehensive treatment of their efficient solutions; Discusses the tradeoff

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between the cost of collecting data and prediction accuracy and provides a methodology for using prior data to reduce cost of data collection in the design, testing and validation of both analog and digital VLSI designs. From the Foreword As the

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semiconductor

*Automation
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*industry embraces the
rising swell of
cognitive systems and
edge intelligence, this
book could serve as a
harbinger and
example of the
osmosis that will exist
between our cognitive
structures and
methods, on the one
hand, and the*

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hardware architectures and technologies that will support them, on the other....As we transition from the computing era to the cognitive one, it behooves us to remember the success story of VLSI CAD and to earnestly seek the help of the

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*invisible hand so that
our future cognitive
systems are used to
design more powerful
cognitive systems. This
book is very much
aligned with this on-
going transition from
computing to
cognition, and it is
with deep pleasure
that I recommend it to
all those who are*

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*actively engaged in
this exciting
transformation. Dr.*

*Ruchir Puri, IBM
Fellow, IBM Watson
CTO & Chief
Architect, IBM T. J.
Watson Research
Center*

*Harnessing VLSI
System Design with
EDA Tools*

From Architectures to

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***Gate-Level Circuits
and FPGAs
Neural Network
Parallel Computing
Chip Design for
Submicron VLSI
Synthesis,
Verification, and Test***

This monograph
is motivated by
the challenges
faced in

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designing reliable VLSI systems in modern VLSI processes. The reliable operation of integrated circuits (ICs) has become increasingly difficult to

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achieve in the deep submicron (DSM) era. With continuously decreasing device feature sizes, combined with lower supply voltages and higher operating frequencies, the noise immunity

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of VLSI circuits is decreasing alarmingly.

Thus, VLSI circuits are becoming more vulnerable to noise effects such as crosstalk, power supply variations, and r

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radiation-induced soft errors. Among these noise sources, soft errors (or error caused by radiation particle strikes) have become an increasingly troublesome

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issue for memory arrays as well as combinational logic circuits. Also, in the DSM era, process variations are increasing at a significant rate, making it more difficult to

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design reliable
VLSI circuits.

Hence, it is
important to
efficiently design
robust VLSI
circuits that are
resilient to
radiation
particle strikes
and process
variations. The

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work presented
in this research
mo- graph
presents several
analysis and
design
techniques with
the goal of
realizing VLSI
circuits, which
are radiation
and process

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variation
tolerant.

Neural Network
Parallel

Computing is
the first book
available to the
professional
market on
neural network
computing for
optimization

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problems. This introductory book is not only for the novice reader, but for experts in a variety of areas including parallel computing, neural network computing,

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computer
science,
communications
, graph theory,
computer aided
design for VLSI
circuits,
molecular
biology,
management
science, and
operations

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research. The goal of the book is to facilitate an understanding as to the uses of neural network models in real-world applications. Neural Network Parallel Computing

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presents a major breakthrough in science and a variety of engineering fields. The computational power of neural network computing is demonstrated by solving

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numerous
problems such
as N-queen,
crossbar switch
scheduling, four-
coloring and k-
colorability,
graph
planarization
and channel
routing, RNA
secondary

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structure
prediction,
knight's tour,
space allocation,
sorting and
searching, and
tiling. Neural
Network Parallel
Computing is an
excellent
reference for
researchers in

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all areas
covered by the
book.

Furthermore,
the text may be
used in a senior
or graduate
level course on
the topic.

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Electrical
Engineering

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Students taking
courses on VLSI
systems, CAD
tools for VLSI,
Design
Automation at
Final Year or
Graduate Level,
Computer
Science courses
on the same
topics, at a

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Practicing
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Engineers

wishing to learn
the state of the
art in VLSI
Design
Automation.
Designers of
CAD tools for
chip design in
software houses

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or large
electronics
companies.

Special

Features: ·

Probably the
first book on
Design

Automation for
VLSI Systems
which covers all
stages of design

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from layout
synthesis
through logic
synthesis to high-
level synthesis.
Clear, precise
presentation of
examples, well
illustrated with
over 200 figures.
Focus on
algorithms for

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tools means it
will appeal to
some Computer
Science as well
as Electrical
Engineering
departments

About The Book:
Enrollments in
VLSI design
automation

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courses are not
large but it's a
very popular

elective,
especially for
those seeking a
career in the
microelectronics
industry.

Already the
reviewers seem
very

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enthusiastic
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about the
coverage of the
book being a
better match for
their courses
than available
competitors,
because it
covers all design
phases. It has
plenty of worked

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problems and a large no. of illustrations. It's a good 'list-builder' title that matches our strategy of focusing on topics that lie on the interface between Elec Eng and

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Science.
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ALGORITHMS
VLSI DESIGN AU
TOMATION John
Wiley & Sons
Analog VLSI
Design
Automation

OBDD -
Foundations and

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Design

Automation
New Data
Structures and
Algorithms for
Logic Synthesis
and Verification
**The summer school on
VLSI GAD Tools and
Applications was held**

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from July 21 through
August 1, 1986 at
Beatenberg in the
beautiful Bernese
Oberland in
Switzerland. The
meeting was given
under the auspices of
IFIP WG 10. 6 VLSI,
and it was sponsored
by the Swiss Federal
Institute of
Technology Zurich,

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Switzerland. Eighty-one professionals were invited to participate in the summer school, including 18 lecturers. The 81 participants came from the following countries:

Australia (1),
Denmark (1), Federal
Republic of Germany
(12), France (3), Italy
(4), Norway (1), South

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Korea (1), Sweden (5),
United Kingdom (1),
United States of
America (13), and
Switzerland (39). Our
goal in the planning
for the summer school
was to introduce the
audience into the
realities of CAD tools
and their applications
to VLSI design. This
book contains articles

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Automation
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by all 18 invited
speakers that lectured
at the summer school.

The reader should
realize that it was not
intended to publish a
textbook. However,
the chapters in this
book are more or less
self-contained
treatments of the
particular subjects.

Chapters 1 and 2 give

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a broad introduction to
Automation
VLSI Design.

Question Papers
Simulation tools and
their algorithmic
foundations are treated
in Chapters 3 to 5 and
17. Chapters 6 to 9
provide an excellent
treatment of modern
layout tools. The use
of CAD tools and
trends in the design of
32-bit microprocessors

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are the topics of
Chapters 10 through
16. Important aspects
in VLSI testing and
testing strategies are
given in Chapters 18
and 19.

This text is about
methods used for the
computer simulation
of analog systems. It
concentrates on
electronic

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applications, but many of the methods are applicable to other engineering problems as well. This revised edition (1st, 1983) encompasses recent theoretical developments and program-writing techniques. This book provides broad and comprehensive

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coverage of the entire
EDA flow. EDA/VLSI
practitioners and
researchers in need of
fluency in an
"adjacent" field will
find this an invaluable
reference to the basic
EDA concepts,
principles, data
structures, algorithms,
and architectures for
the design,

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verification, and test
Automation
of VLSI circuits.

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Anyone who needs to
learn the concepts,
principles, data
structures, algorithms,
and architectures of
the EDA flow will
benefit from this
book. Covers
complete spectrum of
the EDA flow, from
ESL design modeling

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to logic/test synthesis,
verification, physical
design, and test - helps
EDA newcomers to
get "up-and-running"
quickly Includes
comprehensive
coverage of EDA
concepts, principles,
data structures,
algorithms, and
architectures - helps
all readers improve

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their VLSI design
competence Contains
latest advancements
not yet available in
other books, including
Test compression,
ESL design modeling,
large-scale
floorplanning,
placement, routing,
synthesis of clock and
power/ground
networks - helps

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readers to
design/develop
testable chips or
products Includes
industry best-practices
wherever appropriate
in most chapters -
helps readers avoid
costly mistakes
One of Springer's
renowned Major
Reference Works, this
awesome achievement

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provides a comprehensive set of solutions to important algorithmic problems for students and researchers interested in quickly locating useful information.

This first edition of the reference focuses on high-impact solutions from the most recent decade,

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while later editions will widen the scope of the work. All entries have been written by experts, while links to Internet sites that outline their research work are provided. The entries have all been peer-reviewed. This defining reference is published both in print

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and on line.
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VLSI Design and Test
for Systems
Dependability
Analysis and Design
of Resilient VLSI
Circuits
VLSI CAD Tools and
Applications
Machine Intelligence
in Design Automation

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This book teaches the principles of physical design, layout, and simulation of CMOS integrated circuits. It is written around a very powerful CAD program called Microwind that is available

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on the

**accompanying CD-
ROM. Featuring a
friendly
interface,**

**Microwind is both
educational and
useful for
designing CMOS
chips.**

**One of the main
problems in chip
design is the**

enormous number of possible combinations of individual chip elements within a system, and the problem of their compatibility. The recent application of data structures, efficient

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**algorithms, and
ordered binary
decision
diagrams
(OBDDs) has
proven vital in
designing the
computer chips of
tomorrow. This
book provides an
introduction to
the foundations
of this**

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**interdisciplinary
research area,
emphasizing its
applications in
computer aided
circuit design.
This monograph
represents a
summary of our
work in the last
two years in
applying the
method of**

simulated annealing to the solution of problems that arise in the physical design of VLSI circuits. Our study is experimental in nature, in that we are concerned with issues such as solution

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**representations,
neighborhood
structures, cost
functions,
approximation
schemes, and so
on, in order to
obtain good
design results in
a reasonable
amount of com
putation time.**

We hope that our

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**experiences with
the techniques
we employed,
some of which
indeed bear
certain
similarities for
different
problems, could
be useful as hints
and guides for
other researchers
in applying the**

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**method to the
solution of other
problems. Work
reported in this
monograph was
partially
supported by the
National Science
Foundation under
grant MIP
87-03273, by the
Semiconductor
Research**

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**Corporation
under contract
87-DP- 109, by a
grant from the
General Electric
Company, and by
a grant from the
Sandia
Laboratories.
Logic Synthesis
and Verification
Algorithms is a
textbook**

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**designed for
courses on VLSI
Logic Synthesis
and Verification,
Design
Automation, CAD
and advanced
level discrete
mathematics. It
also serves as a
basic reference
work in design
automation for**

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**both
professionals and
students. Logic
Synthesis and
Verification
Algorithms is
about the
theoretical
underpinnings of
VLSI (Very Large
Scale Integrated
Circuits). It
combines and**

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**integrates
modern
developments in
logic synthesis
and formal
verification with
the more
traditional matter
of Switching and
Finite Automata
Theory. The book
also provides
background**

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**material on
Boolean algebra
and discrete
mathematics. A
unique feature of
this text is the
large collection of
solved problems.
Throughout the
text the
algorithms
covered are the
subject of one or**

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**more problems
based on the use
of available
synthesis
programs.
Floorplanning
Algorithms for
VLSI Physical
Design
Automation
Mitigating Soft
Errors and
Process**

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**Variations
Capitalist Nigger
Custom ICs,
FPGAs and GPUs
Algorithms and
Data Structures
in VLSI Design
For the new
millenium,
Wai-Kai Chen
introduced a
monumental**

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**reference for
the design,
analysis, and
prediction of
VLSI circuits:
The VLSI
Handbook.
Still a valuable
tool for
dealing with
the most
dynamic field**

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in
Automation
engineering,
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this second
edition
includes 13
sections
comprising
nearly 100
chapters
focused on the
key concepts,
models, and

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equations.

**Written by a
stellar**

**international
panel of expert
contributors,
this handbook
is a reliable,
comprehensive
resource for
real answers
to practical**

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**problems. It
emphasizes
fundamental
theory
underlying
professional
applications
and also
reflects key
areas of
industrial and
research**

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**focus. WHAT'S
IN THE
SECOND
EDITION?**

Sections on...

**Low-power
electronics
and design**

**VLSI signal
processing**

**Chapters on...
CMOS**

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**fabrication Co
ntent-
addressable
memory
Compound
semiconductor
RF circuits
High-speed
circuit design
principles
SiGe HBT
technology**

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**Bipolar
junction
transistor
amplifiers
Performance
modeling and
analysis using
SystemC
Design
languages,
expanded from
two chapters**

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**to twelve
Testing of
digital systems
Structured for
convenient
navigation and
loaded with
practical
solutions, The
VLSI
Handbook,
Second Edition**

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**remains the
first choice for
answers to the
problems and
challenges
faced daily in
engineering
practice.**

**Genetic
Algorithms
mimic the
natural**

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**process of
evolution,
helping
engineers
optimize their
designs by
using the
principle of
"survival of
the fittest".
VLSI is
especially**

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**suited to
benefit from
genetic
algorithms-
and this
comprehensive
book shows
how to get the
best results.
You will
discover how
genetic**

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algorithms

**work and how
you can use**

**them in a wide
variety of VLSI
design, layout
and test
automation
tasks.**

1156F-7

**Genetic
algorithms**

**mimic the
natural
process of
evolution,
helping
engineers
optimize their
designs by
using the
principle of
"survival of
the fittest."**

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VLSI is especially suited to benefit from genetic algorithms - and this comprehensive book shows you how to get the best results, fast.

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**You'll discover
how genetic
algorithms
work and how
you can use
them in a wide
variety of VLSI
design, layout,
and test
automation
tasks,
including:**

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**Circuit
partitioning
Macro cell**

**routing,
including
Steiner**

**problems and
global routing**

**Standard cell
and macro cell
placement**

Circuit

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**segmentation,
FPGA mapping
and pseudo-
exhaustive
testing
Automatic test
generation
including
compaction, et
erministic/gen
etic test
hybrids and**

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**integration of
finite state
machine
sequences
Peak power
estimation
You'll find
essential
insights into
problem
encoding and
fitness**

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**functions;
coverage of
advanced
parallel imple
mentations;
and much
more. Specific
experimental
results are
presented for
every
application -**

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**as are detailed
problem
descriptions
and easy-to-
adapt
examples.
Genetic
algorithms are
already being
incorporated
into leading
electronic**

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**design
automation
systems.**

**Leverage their
full power now
- with Genetic
Algorithms For
VLSI Design,
Layout, and
Test
Automation.
Single-**

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**threaded
software
applications**

**have ceased to
see significant
gains in p-
formance on a
general-
purpose CPU,
even with
further scaling
in very large**

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**scale
integration
(VLSI)
technology.
This is a
signi?cant
problem for
electronic
design
automation
(EDA)
applications,**

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**since the
design
complexity of
VLSI
integrated
circuits (ICs)
is
continuously
growing. In
this research
monograph,
we evaluate**

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**custom ICs, ?e
ld-
programmable
gate arrays
(FPGAs), and
graphics
processors as
platforms for
accelerating
EDA
algorithms,
instead of the**

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**general-
purpose sing-
threaded CPU.**

**We study
applications
which are used
in key time-
consuming
steps of the
VLSI design
flow. Further,
these**

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**applications
also have
different
degrees of
inherent
parallelism in
them. We
study both con
trol-dominated
EDA
applications
and control**

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**plus data
parallel EDA
applications.**

**We accelerate
these
applications
on these
different
hardware
platforms. We
also present
an automated**

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**approach for
accelerating
certain**

**uniprocessor
applications
on a graphics
processor.**

**This
monograph
compares
custom ICs,
FPGAs, and**

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**graphics
processing
units (GPUs)
as potential
platforms to
accelerate
EDA
algorithms. It
also provides
details of the
programming
model used for**

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**interfacing
with the GPUs.
Handbook of
Algorithms for
Physical
Design
Automation
ALGORITHMS
VLSI DESIGN
AUTOMATION
Computer
Methods for**

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**Circuit
Analysis and
Design
Logic
Synthesis and
Verification
Algorithms
Algorithms For
Vlsi Physical
Design
Automation,
3E**

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This book
presents a
hands-on

approach for
solving
electronic
design

automation
problems with
modern machine
intelligence
techniques by

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including step-
by-step
development of
commercial
grade design
applications
including
resistance
estimation,
capacitance
estimation,
cell

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classification
and others
using dataset
extracted from
designs at
20nm. It walks
the reader
step by step
in building
solution flow
for EDA
problems with

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Python and Ten
sorflow.Intend
ed audience
includes
design
automation
engineers,
managers,
executives,
research
professionals,
graduate

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students,
Machine
learning
enthusiasts,
EDA and CAD
developers,
mentors, and
the merely
inquisitive.

It is
organized to
serve as a

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compendium to
a beginner, a
ready

reference to
intermediate
and source for
an expert.

The physical
design flow of
any project
depends upon
the size of

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the design,
the
technology,
the number of
designers, the
clock
frequency, and
the time to do
the design. As
technology
advances and
design-styles

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change,
physical
design flows
are constantly
reinvented as
traditional
phases are
removed and
new ones are
added to
accommodate
changes in

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technology.
Handbook of
Algorithms for
Physical
Design
Automation
provides a
detailed
overview of
VLSI physical
design
automation,

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emphasizing state-of-the-art techniques, trends and improvements that have emerged during the previous decade. After a brief introduction to the modern

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physical
design
problem, basic
algorithmic
techniques,
and
partitioning,
the book
discusses
significant
advances in
floorplanning

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representation
s and
describes
recent
formulations
of the
floorplanning
problem. The
text also
addresses
issues of
placement, net

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layout and
optimization,
routing
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signal nets, m
anufacturabili
ty, physical
synthesis,
special nets,
and designing
for
specialized

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technologies.
It includes a
personal
perspective
from Ralph
Otten as he
looks back on
the major
technical
milestones in
the history of
physical

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design
automation.
Although
several books
on this topic
are currently
available,
most are
either too
broad or out
of date.

Alternatively,

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proceedings
and journal
articles are
valuable
resources for
researchers in
this area, but
the material
is widely
dispersed in
the
literature.

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This handbook
pulls together
a broad

variety of
perspectives
on the most
challenging
problems in
the field, and
focuses on
emerging
problems and

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research
Automation
results.
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Covers the
statistical
analysis and
optimization
issues arising
due to
increased
process
variations in
current

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technologies.
Comprises a
valuable
reference for
statistical
analysis and
optimization
techniques in
current and
future VLSI
design for CAD-
Tool

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developers and
for
researchers
interested in
starting work
in this very
active area of
research.

Written by
author who
lead much
research in

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this area who provide novel ideas and approaches to handle the addressed issues

With the proliferation of VHDL, the reference material also

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grew in the
same order.

Today there is
good amount of
scholarly
literature
including many
books
describing
various
aspects of
VHDL. However,

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an indepth
review of
these books
reveals a
different
story. Many of
them have
emerged simply
as an improved
version of the
manual. While
some of them

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deal with the system design issues, they lack

appropriate exemplifying to illustrate the concepts.

Others give large number of examples, but lack the

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VLSI system design issues. In nutshell, the fact which gone unnoticed by most of the books, is the growth of the VLSI is not merely due to the language itself, but

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more due to
the
development of
large number
of third party
tools useful
from the FPGA
or semicustom
ASIC
realization
point of view.
In the

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proposed book,
the authors
have

synergized the
VHDL
programming
with
appropriate
EDA tools so
as to present
a full proof
system design

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to the
readers. In
this book
along with the
VHDL coding
issues, the
simulation and
synthesis with
the various
toolsets
enables the
potential

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reader to
visualize the
final design.

The VHDL
design codes
have been
synthesized
using
different
third party
tools such as
Xilinx Web

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pack Ver.11,
Modelsim PE,
Leonrado
Spectrum and
Synplify Pro.
Mixed flow
illustrated by
using the
above
mentioned
tools presents
an insight to

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optimize the
design with
reference to
the spatial,
temporal and
power metrics.

Hardware
Acceleration
of EDA
Algorithms
Encyclopedia
of Algorithms

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VLSI Design
Methodology
Development
The Road To
Success – A
Spider Web
Doctrine
EDA for IC Imp
lementation,
Circuit
Design, and
Process

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Technology
Algorithms for VLSI
Physical Design
Automation is a
core reference text
for graduate
students and CAD
professionals. It
provides a
comprehensive
treatment of the
principles and
algorithms of VLSI

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physical design.
Algorithms for VLSI
Physical Design
Automation
presents the
concepts and
algorithms in an
intuitive manner.
Each chapter
contains 3-4
algorithms that are
discussed in detail.
Additional

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algorithms are presented in a somewhat shorter format. References to advanced algorithms are presented at the end of each chapter. Algorithms for VLSI Physical Design Automation covers all aspects of physical design. The

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first three chapters provide the background material while the subsequent chapters focus on each phase of the physical design cycle. In addition, newer topics like physical design automation of FPGAs and MCMs

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have been included.
The author provides
an extensive
bibliography which
is useful for finding
advanced material
on a topic.

Algorithms for VLSI
Physical Design
Automation is an
invaluable
reference for
professionals in

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layout, design
automation and
physical design.

Capitalist Nigger is
an explosive and
jarring indictment
of the black race.

The book asserts
that the Negroid
race, as naturally
endowed as any
other, is culpably a
non-productive

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race, a consumer
race that depends
on other

communities for its
culture, its
language, its
feeding and its
clothing. Despite
enormous natural
resources, blacks
are economic slaves
because they lack
the ' devil-may-

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care ' attitude and
the ' killer
instinct ' of the
Caucasian, as well
as the spider web
mentality of the
Asian. A Capitalist
Nigger must
embody
ruthlessness in
pursuit of
excellence in his
drive towards

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achieving the goal
of becoming an
economic warrior.

In putting forward
the idea of the
Capitalist Nigger,
Chika Onyeani
charts a road to
success whereby
black economic
warriors employ the
' Spider Web
Doctrine ' –

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discipline, self-reliance, ruthlessness – to escape from their victim mentality.

Born in Nigeria, Chika Onyeani is a journalist, editor and former diplomat.

This book introduces new logic primitives for

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electronic design
automation tools.
The author
approaches
fundamental EDA
problems from a
different,
unconventional
perspective, in
order to
demonstrate the
key role of
rethinking EDA

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solutions in overcoming technological limitations of present and future technologies. The author discusses techniques that improve the efficiency of logic representation, manipulation and optimization tasks

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by taking
advantage of
majority and
biconditional logic
primitives. Readers
will be enabled to
accelerate formal
methods by
studying core
properties of logic
circuits and
developing new
frameworks for

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logic reasoning
Automation
engines.

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Very Large Scale

Integration (VLSI)

Systems refer to the
latest development
in computer

microchips which

are created by

integrating

hundreds of

thousands of

transistors into one

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chip. Emerging research in this area has the potential to uncover further applications for VLSI technologies in addition to system advancements.

Design and Modeling of Low Power VLSI Systems analyzes various traditional and

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modern low power techniques for integrated circuit design in addition to the limiting factors of existing techniques and methods for optimization.

Through a research-based discussion of the technicalities involved in the VLSI

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hardware
development
process cycle, this
book is a useful
resource for
researchers,
engineers, and
graduate-level
students in
computer science
and engineering.
CMOS Layout and
Simulation

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Algorithms for the
Layout Problem in
VLSI Design
Automation
Theory and Practice
Machine Learning
in VLSI Computer-
Aided Design
VLSI Physical
Design Automation
Top-Down VLSI
Design: From
Architectures to

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Gate-Level Circuits
and FPGAs

represents a unique approach to learning digital design.

Developed from more than 20 years teaching circuit design, Doctor Kaeslin's approach follows the natural VLSI design flow and makes circuit design accessible

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for professionals with a background in systems engineering or digital signal processing. It begins with hardware architecture and promotes a system-level view, first considering the type of intended application and

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letting that guide your design choices. Doctor Kaeslin presents modern considerations for handling circuit complexity, throughput, and energy efficiency while preserving functionality. The book focuses on application-specific

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integrated circuits (ASICs), which along with FPGAs are increasingly used to develop products with applications in telecommunications, IT security, biomedical, automotive, and computer vision industries. Topics include field-

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programmable logic,
algorithms,
verification,
modeling hardware,
synchronous
clocking, and more.
Demonstrates a top-
down approach to
digital VLSI design.
Provides a
systematic overview
of architecture
optimization
techniques.

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Features a chapter on field-programmable logic devices, their technologies and architectures.

Includes checklists, hints, and warnings for various design situations.

Emphasizes design flows that do not overlook important action items and

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which include
alternative options
when planning the
development of
microelectronic
circuits.

&Quot;VLSI
Physical Design
Automation: Theory
and Practice is an
essential
introduction for
senior
undergraduates,

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postgraduates and
anyone starting
work in the field of

CAD for VLSI. It
covers all aspects of
physical design,
together with such
related areas as
automatic cell
generation, silicon
compilation, layout
editors and
compaction. A
problem-solving

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approach is adopted
and each solution is
illustrated with

examples. Each
topic is treated in a
standard format:

Problem Definition,
Cost Functions and
Constraints,
Possible

Approaches and
Latest Development
s."--BOOK JACKET.

Very Large Scale

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Integration (VLSI)

has become a
necessity rather
than a specialization
for electrical and
computer engineers.

This unique text
provides
Engineering and
Computer Science
students with a
comprehensive
study of the subject,
covering VLSI from

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basic design
techniques to
working principles
of physical design
automation tools to
leading edge
application-specific
array processors.
Beginning with
CMOS design, the
author describes
VLSI design from
the viewpoint of a
digital circuit

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engineer. He develops physical pictures for CMOS circuits and demonstrates the top-down design methodology using two design projects - a microprocessor and a field programmable gate array. The author then discusses VLSI testing and

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dedicates an entire chapter to the working principles, strengths, and weaknesses of ubiquitous physical design tools. Finally, he unveils the frontiers of VLSI. He emphasizes its use as a tool to develop innovative algorithms and architecture to solve

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previously
intractable

problems. VLSI

Design answers not only the question of "what is VLSI," but also shows how to use VLSI. It provides graduate and upper level undergraduate students with a complete and congregated view of VLSI engineering.

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Practical Problems
Automation
in VLSI Physical

Design Automation

contains problems
and solutions

related to various
well-known

algorithms used in
VLSI physical

design automation.

Dr. Lim believes that
the best way to learn
new algorithms is to
walk through a small

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example by hand. This knowledge will greatly help understand, analyze, and improve some of the well-known algorithms. The author has designed and taught a graduate-level course on physical CAD for VLSI at Georgia Tech. Over the years he has

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written his
homework with such
a focus and has
maintained typeset
version of the
solutions.

Algorithms for VLSI
Physical Design
Automation
Logic Synthesis and
Verification
VLSI Design
The VLSI Handbook
Genetic Algorithms:

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Layout & Test
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This book
discusses the new
roles that the VLSI
(very-large-scale
integration of
semiconductor
circuits) is taking
for the safe,
secure, and

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dependable design and operation of electronic systems. The book consists of three parts. Part I, as a general introduction to this vital topic, describes how electronic systems

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are designed and
tested with
particular

emphasis on
dependability
engineering,
where the
simultaneous
assessment of the
detrimental
outcome of
failures and cost

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of their
containment is
made. This section
also describes the
related research
project

“Dependable VLSI
Systems,” in
which the editor
and authors of the
book were
involved for 8

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years. Part II
addresses various
threats to the
dependability of
VLSIs as key
systems
components,
including time-
dependent
degradations,
variations in
device

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characteristics,
ionizing radiation,
electromagnetic
interference,
design errors, and
tampering, with
discussion of
technologies to
counter those
threats. Part III
elaborates on the
design and test

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technologies for dependability in such applications as control of robots and vehicles, data processing, and storage in a cloud environment and heterogeneous wireless telecomm unications. This

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book is intended to be used as a reference for engineers who work on the design and testing of VLSI systems with particular attention to dependability. It can be used as a textbook in

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graduate courses as well. Readers interested in dependable systems from social and industrial-economic perspectives will also benefit from the discussions in this book.

This book provides

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some recent
advances in
design nanometer
VLSI chips. The
selected topics try
to present some
open problems
and challenges
with important
topics ranging
from design tools,
new post-silicon

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devices, GPU-based parallel computing, emerging 3D integration, and antenna design. The book consists of two parts, with chapters such as: VLSI design for multi-sensor smart systems on

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a chip, Three-
dimensional
integrated circuits
design for
thousand-core
processors,
Parallel symbolic
analysis of large
analog circuits on
GPU platforms,
Algorithms for
CAD tools VLSI

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design, A
multilevel
memetic
algorithm for large
SAT-encoded
problems, etc.
The Complete,
Modern Tutorial
on Practical VLSI
Chip Design,
Validation, and
Analysis As

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microelectronics
engineers design
complex chips
using existing
circuit libraries,
they must ensure
correct logical,
physical, and
electrical
properties, and
prepare for
reliable foundry

fabrication. VLSI
Design
Methodology
Development
focuses on the
design and
analysis steps
needed to perform
these tasks and
successfully
complete a
modern chip

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design.

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Microprocessor
design authority

Tom Dillinger
carefully

introduces core
concepts, and
then guides
engineers through
modeling,
functional design
validation, design

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implementation,
electrical analysis,
and release to
manufacturing.
Writing from the
engineer's
perspective, he
covers underlying
EDA tool
algorithms, flows,
criteria for
assessing project

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status, and key tradeoffs and interdependencies . This fresh and accessible tutorial will be valuable to all VLSI system designers, senior undergraduate or graduate students of microelectronics

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design, and
companies
offering internal
courses for
engineers at all
levels. Reflect
complexity, cost,
resources, and
schedules in
planning a chip
design project
Perform

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hierarchical
design
decomposition,
floorplanning, and
physical
integration,
addressing DFT,
DFM, and DFY
requirements
Model
functionality and
behavior, validate

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designs, and
verify formal
equivalency Apply
EDA tools for logic
synthesis,
placement, and
routing Analyze
timing, noise,
power, and
electrical issues
Prepare for
manufacturing

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release and bring-up, from mastering ECOs to qualification This guide is for all VLSI system designers, senior undergraduate or graduate students of microelectronics design, and

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time logic to GDSII (a file format used to transfer data of semiconductor physical layout), analog/mixed signal design, physical verification, and technology CAD (TCAD). Chapters contributed by

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The explosive

growth and

development of

the integrated

*circuit market
over the last
few years have
been mostly
limited to the
digital VLSI
domain. The
difficulty of
automating the
design process
in the analog
domain, the*

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*fact that a
general analog
design
methodology
remained
undefined, and
the poor
performance of
earlier tools
have left the
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