Arm Corelink Mmu 500 System Memory Management Unit

Offers users the first resource guide that combines both the methodology and basics of SystemVerilog Addresses how all these pieces fit together and how they should be used to verify complex chips rapidly and thoroughly. Unique in its broad coverage of SystemVerilog, advanced functional verification, and the combination of the two.

About the ARM Architecture The ARM architecture is the industry's leading 16/32-bit embedded RISC processor solution. ARM Powered microprocessors are being routinely designed into a wider range of products than any other 32-bit processor. This wide applicability is made possible by the ARM architecture, resulting in optimal system solutions at the crossroads of high performance, low power consumption and low cost. About the book This is the authoritative reference guide to the ARM RISC architecture. Produced by the architects that are actively working on the ARM specification, the book contains detailed information about all versions of the ARM and Thumb instruction sets, the memory management and cache functions, as well as optimized code examples. 0201737191B05092001

This new edition has been fully revised and updated to include extensive information on the ARM Cortex-M4 processor, providing a complete up-to-date guide to both Cortex-M3 and Cortex-M4 processors, and which enables migration from various processor architectures to the exciting world of the Cortex-M3 and M4. This book presents the background of the ARM architecture and outlines the features of the processors such as the instruction set, interrupt-handling and also demonstrates how to program and utilize the advanced features available such as the Memory Protection Unit (MPU). Chapters on getting started with IAR, Keil, gcc and CooCox CoIDE tools help beginners develop program codes. Coverage also includes the important areas of software development such as using the low power features, handling information input/output, mixed language projects with assembly and C, and other advanced topics. Two new chapters on DSP features and CMSIS-DSP software libraries, covering DSP fundamentals and how to write DSP software for the Cortex-M4 processor, including examples of using the CMSIS-DSP library, as well as useful information about the DSP capability of the Cortex-M4 processor A new chapter on the Cortex-M4 floating point unit and how to use it A new chapter on using embedded OS (based on CMSIS-RTOS), as well as details of processor features to support OS operations Various debugging techniques as well as a troubleshooting guide in the appendix topics on software porting from other architectures A full range of easy-to-understand examples, diagrams and quick reference appendices

This book introduces the Zynq MPSoC (Multi-Processor System-on-Chip), an embedded device from Xilinx. The Zynq MPSoC combines a sophisticated processing system that includes ARM Cortex-A53 applications and ARM Cortex-R5 real-time processors, with FPGA programmable logic. As well as guiding the reader through the architecture of the device, design tools and methods are also covered in detail: both the conventional hardware/software co-design approach, and the newer software-defined methodology using Xilinx's SDx development environment. Featured aspects of Zynq MPSoC design include hardware and software development, multiprocessing, safety, security and platform management, and system booting. There are also special features on PYNQ, the Python-based framework for Zynq devices, and machine learning applications. This book should serve as a useful guide for those working with Zynq MPSoC, and equally as a reference for technical managers wishing to gain familiarity with the device and its associated design methodologies.

Designing 2D and 3D Network-on-Chip Architectures

Cache, DRAM, Disk

Embedded Computing

The Definitive Guide to the ARM Cortex-M3

Unique Chips and Systems

The refereed proceedings of the 12th Asia-Pacific Computer Systems Architecture Conference are presented in this volume. Twenty-six full papers are presented together with two keynote and eight invited lectures. Collectively, they represent some of the most important developments in computer systems architecture. The papers emphasize hardware and software techniques for state-of-the-art, multi-core and multi-threaded architectures.

The fact that there are more embedded computers than general-purpose computers and that we are impacted by hundreds of them every day is no longer news. What is news is that their increasing performance requirements, complexity and capabilities demand a new approach to their design. Fisher, Faraboschi, and Young describe a new age of embedded computing design, in which the processor is central, making the approach radically distinct from contemporary practices of embedded systems design. They demonstrate why it is essential to take a computing-centric and system-design approach to the traditional elements of nonprogrammable components, peripherals, interconnects and buses. These elements must be unified in a system design with high-performance processor architectures, microarchitectures and compilers, and with the compilation tools, debuggers and simulators needed for application development. In this landmark text, the authors apply their expertise in highly interdisciplinary hardware/software development and VLIW processors to illustrate this change in embedded computing. VLIW architectures have long been a popular choice in embedded systems design, and while VLIW is a running theme throughout the book, embedded computing is the core topic. Embedded Computing examines both in a book filled with fact and opinion based on the authors many years of R&D experience. · Complemented by a unique, professional-quality embedded tool-chain on the authors' website, http://www.vliw.org/book · Combines technical depth with real-world experience · Comprehensively explains the differences between general purpose computing systems and embedded systems at the hardware, software, tools and operating system levels. · Uses concrete examples to explain and motivate the trade-offs.

This 1995 edition features datasheets for the embedded Intel386 processor family. It is the source for complete product specifications, datasheets and architecture descriptions for the Intel386 processors, as well as Intel376 processors and peripherals and the industry standard for 16-bit designs--the 80186/80188 family.

Dynamically Reconfigurable Systems is the first ever to focus on the emerging field of Dynamically Reconfigurable Computing Systems. While programmable logic and design-time configurability are well elaborated and covered by various texts, this book presents a unique overview over the state of the art and recent results for dynamic and run-time reconfigurable computing systems. Reconfigurable hardware is not only of utmost importance for large manufacturers and vendors of microelectronic devices and systems, but also a very attractive technology for smaller and medium-sized companies. Hence, Dynamically Reconfigurable Systems also addresses researchers and engineers actively working in the field and provides them with information on the newest developments and trends in dynamic and run-time reconfigurable systems.

Arm System-On-Chip Architecture, 2/E

Verification Methodology Manual for SystemVerilog

FPGA-based Prototyping Methodology Manual

Exploring Zynq Mpsoc

The Zynq Book

STRUCTURED COMPUTER ORGANIZATION

Many modern computer systems, including homogeneous and heterogeneous architectures, support shared memory in hardware. In a shared memory system, each of the processor cores may read and write to a single shared address space. For a shared memory machine, the memory consistency model defines the architecturally visible behavior of its memory system. Consistency definitions provide rules about loads and stores (or memory reads and writes) and how they act upon memory. As part of supporting a memory consistency model, many machines also provide cache coherence protocols that ensure that multiple cached copies of data are kept up-to-date. The goal of this primer is to provide readers with a basic understanding of consistency and coherence. This understanding includes both the issues that must be solved as well as a variety of solutions. We present both high-level concepts as well as specific, concrete examples from real-world systems. This second edition reflects a decade of advancements since the first edition and includes, among other more modest changes, two new chapters: one on consistency and coherence for non-CPU accelerators (with a focus on GPUs) and one that points to formal work and tools on consistency and coherence.

The push to move products to market as quickly and cheaply as possible is fiercer than ever, and accordingly, engineers are always looking for new ways to provide their companies with the edge over the competition. Field-Programmable Gate Arrays (FPGAs), which are faster, denser, and more cost-effective than traditional programmable logic devices (PLDs), are quickly becoming one of the most widespread tools that embedded engineers can utilize in order to gain that needed edge. FPGAs are especially popular for prototyping designs, due to their superior speed and efficiency. This book hones in on that rapid prototyping aspect of FPGA use, showing designers exactly how they can cut time off production cycles and save their companies money drained by costly mistakes, via prototyping designs with FPGAs first. Reading it will take a designer with a basic knowledge of implementing FPGAs to the “next-level of FPGA use because unlike broad beginner books on FPGAs, this book presents the required design skills in a focused, practical, example-oriented manner. In-the-trenches expert authors assure the most applicable advice to practicing engineers Dual focus on successfully making critical decisions and avoiding common pitfalls appeals to engineers pressured for speed and perfection Hardware and software are both covered, in order to address the growing trend toward "cross-pollination" of engineering expertise

Hardware/software co-verification is how to make sure that embedded system software works correctly with the hardware, and that the hardware has been properly designed to run the software successfully -before large sums are spent on prototypes or manufacturing. This is the first book to apply this verification technique to the rapidly growing field of embedded systems-on-a-chip(SoC). As traditional embedded system design evolves into single-chip design, embedded engineers must be armed with the necessary information to make educated decisions about which tools and methodology to deploy. SoC verification requires a mix of expertise from the disciplines of microprocessor and computer architecture, logic design and simulation, and C and Assembly language embedded software. Until now, the relevant information on how it all fits together has not been available. Andrews, a recognized expert, provides in-depth information about how co-verification really works, how to be successful using it, and pitfalls to avoid. He illustrates these concepts using concrete examples with the ARM core - a technology that has the dominant market share in embedded system product design. The companion CD-ROM contains all source code used in the design examples, a searchable e-book version, and useful design tools. * The only book on verification for systems-on-a-chip (SoC) on the market * Will save engineers and their companies time and money by showing them how to speed up the testing process, while still avoiding costly mistakes * Design examples use the ARM core, the dominant technology in SoC, and all the source code is included on the accompanying CD-Rom, so engineers can easily use it in their own designs

Is your memory hierarchy stopping your microprocessor from performing at the high level it should be? Memory Systems: Cache, DRAM, Disk shows you how to resolve this problem. The book tells you everything you need to know about the logical design and operation, physical design and operation, performance characteristics and resulting design trade-offs, and the energy consumption of modern memory hierarchies. You learn how to to tackle the challenging optimization problems that result from the side-effects that can appear at any point in the entire hierarchy. As a result you will be able to design and emulate the entire memory hierarchy. Understand all levels of the system hierarchy -Xcache, DRAM, and disk. Evaluate the system-level effects of all design choices. Model performance and energy consumption for each component in the memory hierarchy.

Embedded Systems Foundations of Cyber-Physical Systems

Instructor guide

Accelerating the Design Process

EMBEDDED SYSTEM DESIGN

Embedded Systems Hardware for Software Engineers

An Illustrated Introduction to Microprocessors and Computer Architecture

The Definitive Guide to the ARM Cortex-M0 is a guide for users of ARM Cortex-M0 microcontrollers. It presents many examples to make it easy for novice embedded-software developers to use the full 32-bit ARM Cortex-M0 processor. It provides an overview of ARM and ARM processors and discusses the benefits of ARM Cortex-M0 over 8-bit or 16-bit devices in terms of energy efficiency, code density, and ease of use, as well as their features and applications. The book describes the architecture of the Cortex-M0 processor and the programmers model, as well as Cortex-M0 programming and instruction set and how these instructions are used to carry out various operations. Furthermore, it considers how the memory architecture of the Cortex-M0 processor affects software development; Nested Vectored Interrupt Controller (NVIC) and the features it supports, including flexible interrupt management, nested interrupt support, vectored exception entry, and interrupt masking; and Cortex-M0 features that target the embedded operating system. It also explains how to develop simple applications on the Cortex-M0, how to program the Cortex-M0 microcontrollers in assembly and mixed-assembly languages, and how the low-power features of the Cortex-M0 processor are used in programming. Finally, it describes a number of ARM Cortex-M0 products, such as microcontrollers, development boards, starter kits, and development suites. This book will be useful to both new and advanced users of ARM Cortex devices, from students and hobbyists to researchers, professional embedded- software developers, electronic enthusiasts, and even semiconductor product designers. The first and definitive book on the new ARM Cortex-M0 architecture targeting the large 8-bit and 16-bit microcontroller market Explains the Cortex-M0 architecture and how to program it using practical examples Written by an engineer at ARM who was heavily involved in its development

This book provides readers with an overview of the architectures, programming frameworks, and hardware accelerators for typical cloud computing applications in data centers. The authors present the most recent and promising solutions, using hardware accelerators to provide high throughput, reduced latency and higher energy efficiency compared to current servers based on commodity processors. Readers will benefit from state-of-the-art information regarding application requirements in contemporary data centers, computational complexity of typical tasks in cloud computing, and a programming framework for the efficient utilization of the hardware accelerators.

This user's guide does far more than simply outline the ARM Cortex-M3 CPU features; it explains step-by-step how to program and implement the processor in real-world designs. It teaches readers how to utilize the complete and thumb instruction sets in order to obtain the best functionality, efficiency, and reuseability. The author, an ARM engineer who helped develop the core, provides many examples and diagrams that aid understanding. Quick reference appendices make locating specific details a snap! Whole chapters are dedicated to: Debugging using the new CoreSight technology Migrating effectively from the ARM7 The Memory Protection Unit Interfaces, Exceptions,Interrupts ...and much more! The only available guide to programming and using the groundbreaking ARM Cortex-M3 processor Easy-to-understand examples, diagrams, quick reference appendices, full instruction and Thumb-2 instruction sets are included T teaches end users how to start from the ground up with the M3, and how to migrate from the ARM7

Heterogeneous systems on chip (HeSoCs) combine general-purpose, feature-rich multi-core host processors with domain-specific programmable many-core accelerators (PMCAs) to unite versatility with energy efficiency and peak performance. By virtue of their heterogeneity, HeSoCs hold the promise of increasing performance and energy efficiency compared to homogeneous multiprocessors, because applications can be executed on hardware that is designed for them. However, this heterogeneity also increases system complexity substantially. This thesis presents the first research platform for HeSoCs where all components, from accelerator cores to application programming interface, are available under permissive open-source licenses. We begin by identifying the hardware and software components that are required in HeSoCs and by designing a representative hardware and software architecture. We then design, implement, and evaluate four critical HeSoC components that have not been discussed in research at the level required for an open-source implementation: First, we present a modular, topology-agnostic, high-performance on-chip communication platform, which adheres to a state-of-the-art industry-standard protocol. We show that the platform can be used to build high-bandwidth (e.g., 2.5 GHz and 1024 bit data width) end-to-end communication fabrics with high degrees of concurrency (e.g., up to 256 independent concurrent transactions). Second, we present a modular and efficient solution for implementing atomic memory operations in highly-scalable many-core processors, which demonstrates near-optimal linear throughput scaling for various synthetic and real-world workloads and requires only 0.5 kGE per core. Third, we present a hardware-software solution for shared virtual memory that avoids the majority of translation lookaside buffer misses with prefetching, supports parallel burst transfers without additional buffers, and can be scaled with the workload and number of parallel processors. Our work improves accelerator performance for memory-intensive kernels by up to 4×. Fourth, we present a software toolchain for mixed-data-model heterogeneous compilation and OpenMP offloading. Our work enables transparent memory sharing between a 64-bit host processor and a 32-bit accelerator at overheads below 0.7 % compared to 32-bit-only execution. Finally, we combine our contributions to a research platform for state-of-the-art HeSoCs and demonstrate its performance and flexibility.

System-on-Chip Design with Arm® Cortex®-M Processors

Hardware Accelerators in Data Centers

Inside the Machine

Embedded Software for SoC

Advances in Computer Systems Architecture

IPC-2591, Version 1.4 - Connected Factory Exchange (CFX)

*The design of today's semiconductor chips for various applications, such as telecommunications, poses various challenges due to the complexity of these systems. These highly complex systems-on-chips demand new approaches to connect and manage the communication between on-chip processing and storage components and networks on chips (NoCs) provide a powerful solution. This book is the first to provide a unified overview of NoC technology. It includes in-depth analysis of all the on-chip communication challenges, from physical wiring implementation up to software architecture, and a complete classification of their various Network-on-Chip approaches and solutions. * Leading-edge research from world-renowned experts in academia and industry with state-of-the-art technology implementations/trends * An integrated presentation not currently available in any other book * A thorough introduction to current design methodologies and chips designed with NoCs*

Designing a complex ASIC/SoC is similar to learning a new language to start with and ultimately creating a masterpiece using experience, imagination, and creativity. Digital design starts with RTL such as Verilog or VHDL, but it is only the beginning. A complete designer needs to have a good understanding of the Verilog language, digital design techniques, system architecture, IO protocols, and hardware-software interaction. Some of it will come from experience, and some will come with concerted effort. Graduating from college and entering into the world of digital system design becomes an overwhelming task, as not all the information is readily available. In this book, we have made an effort to explain the concepts in a simple way with real-world examples in Verilog. The book is intended for digital and system design engineers with emphasis on design and system architecture. The book is broadly divided into two sections - chapters 1 through 10, focusing on the digital design aspects and chapters 11 through 20, focusing on the system aspects of chip design. This book can be used by students taking digital design and chip design courses in college and availing it as a guide in their professional careers. Chapter 3 focuses on the synthesizable Verilog constructs, with examples on reusable design (parameterized design, functions, and generate structure). Chapter 5 describes the basic concepts in digital design - logic gates, truth table, De Morgan's theorem, set-up and hold time, edge detection, and number system. Chapter 6 goes into details of digital design explaining larger building blocks such as LFSR, scrambler/descramblers, error detection and correction, parity, CRC, Gray encoding/decoding, priority encoders, 8b/10b encoding, data converters, and synchronization techniques. Chapter 7 and 8 bring in advanced concepts in chip design and architecture - clocking and reset strategy, methods to increase throughput and reduce latency, flow-control mechanisms, pipeline operation, out-of-order execution, FIFO design, state machine design, arbitration, bus interfaces, linked list structure, and LRU usage and implementation. Chapter 9 and 10 describe how to build and design ASIC/SoC. It talks about chip micro-architecture, portioning, datapath, control logic design, and other aspects of chip design such as clock tree, reset tree, and EEPROM. It also covers good design practices, things to avoid and adopt, and best practices for high-speed design. The second part of the book is devoted to System architecture, design, and IO protocols. Chapter 11 talks about memory, memory hierarchy, cache, interrupt, types of DMA and DMA operation. There is Verilog RTL for a typical DMA controller design that explains the scatter-gather DMA concept. Chapter12 describes hard drive, solid-state drive, DDR operation, and other parts of a system such as BIOS, OS, drivers, and their interaction with hardware. Chapter 13 describes embedded systems and internal buses such as AHB, AXI used in embedded design. It describes the concept of transparent and non-transparent bridging. Chapter 14 and chapter 15 bring in practical aspects of chip development - testing, DFT, scan, ATPG, and detailed flow of the chip development cycle (Synthesis, Static timing, and ECO). Chapter 16 and chapter 17 are on power saving and power management protocols. Chapter 16 has a detailed description of various power savings techniques (frequency variation, clock gating, and power well isolation). Chapter 17 talks about Power Management protocols such as system S states, CPU C states, and device D states. Chapter 18 explains the architecture behind serial-bus technology, PCS, and PMA layer. It describes clocking architecture and advanced concepts such as elasticity FIFO, channel bonding (deskewing), link aggregation, and lane reversal. Chapter 19 and 20 are devoted to serial bus protocols (PCI Express, Serial ATA, USB, Thunderbolt, and Ethernet) and their operation.

Most people know that there are 70 million Baby Boomers in America today....but what is less known is that there are approximately 100 million people in America between the ages of 16 and 30. This generation has just entered, or will soon be entering the work force. And they have no idea how to invest, save, or handle their money. Young people today come out of school having had little or no formal education on the basics of money management. Many have large debts from student loans looming over their heads. And many feel confused and powerless when their pricey educations don't translate into high paying jobs. They feel that their $30,000-$40,000 salary is too meager to bother with investing, and they constantly fear that there will be "too much month left at the end of their money." Douglas R. Andrew has shown the parents of this generation a different pathway to financial freedom. Now Doug and his sons, Emron and Aaron - both of whom are in their mid-20s - show the under-30 crowd how they can break from traditional 401k investment plans and instead can find a better way by investing in real estate, budgeting effectively, avoiding unnecessary taxes and using life insurance to create tax-free income. With the principles outlined in Millionaire by Thirty, recent graduates will be earning enough interest on their savings to meet their basic living expenses by the time they're 30. And by the time they're 35, their investments will be earning more money than they are, guaranteeing them a happy, wealthy future.

This book collects the best practices FPGA-based Prototyping of SoC and ASIC devices into one place for the first time, drawing upon not only the authors' own knowledge but also from leading practitioners worldwide in order to present a snapshot of best practices today and possibilities for the future. The book is organized into chapters which appear in the same order as the tasks and decisions which are performed during an FPGA-based prototyping project. We start by analyzing the challenges and benefits of FPGA-based Prototyping and how they compare to other prototyping methods. We present the current state of the available FPGA technology and tools and how to get started on a project. The FPMM also compares between home-made and outsourced FPGA platforms and how to analyze which will best meet the needs of a given project. The central chapters deal with implementing an SoC design in FPGA technology including clocking, conversion of memory, partitioning, multiplexing and handling IP amongst many other subjects. The important subject of bringing up the design on the FPGA boards is covered next, including the introduction of the real design into the board, running embedded software upon it in and debugging and iterating in a lab environment. Finally we explore how the FPGA-based Prototype can be linked into other verification methodologies, including RTL simulation and virtual models in SystemC. Along the way, the reader will discover that an adoption of FPGA-based Prototyping from the beginning of a project, and an approach we call Design-for-Prototyping, will greatly increase the success of the prototype and the whole SoC project, especially the embedded software portion. Design-for-Prototyping is introduced and explained and promoted as a manifesto for better SoC design. Readers can approach the subjects from a number of directions. Some will be experienced with many of the tasks involved in FPGA-based Prototyping but are looking for new insights and ideas; others will be relatively new to the subject but experienced in other verification methodologies; still others may be project leaders who need to understand if and how the benefits of FPGA-based prototyping apply to their next SoC project. We have tried to make each subject chapter relatively standalone, or where necessary, make numerous forward and backward references between subjects, and provide recaps of certain key subjects. We hope you like the book and we look forward to seeing you on the FPMM on-line community soon (go to www.synopsys.com/fpmm).

Phase-coded Pulse Compression

Textbook

ARM Architecture Reference Manual

Low Power Methodology Manual

Operating Systems Foundations with Linux on the Raspberry Pi

12th Asia-Pacific Conference, ACSAC 2007, Seoul, Korea, August 23-25, 2007, Proceedings

Embedded system, as a subject, is an amalgamation of different domains, such as digital design, architecture, operating systems, interfaces, and algorithmic optimization techniques. This book acquaints the students with the alternatives and intricacies of embedded system design. It is designed as a textbook for the undergraduate students of Electronics and Communication Engineering, Electronics and Instrumentation Engineering, Computer Science and Engineering, Information Communication Technology (ICT), as well as for the postgraduate students of Computer Applications (MCA). While in the hardware platform the book explains the role of microcontrollers and introduces one of the most widely used embedded processor, ARM, it also deliberates on other alternatives, such as digital signal processors, field programmable devices, and integrated circuits. It provides a very good overview of the interfacing standards covering RS232C, RS422, RS485, USB, IrDA, Bluetooth, and CAN. In the software domain, the book introduces the features of real-time operating systems for use in embedded applications. Various scheduling algorithms have been discussed with their merits and demerits. The existing real-time operating systems have been surveyed. Guided by cost and performance requirements, embedded applications are often implemented partly in hardware and partly in software. The book covers the different optimization techniques proposed in the literature to take a judicious decision about this partitioning of application tasks. Power-aware design of embedded systems has also been dealt with. In its second edition, the text has been extensively revised and updated. Almost all the chapters have been modified and elaborated including detailed discussion on hardware platforms—ARM, DSP, and FPGA. The chapter on "interfacing standards" has been updated to incorporate the latest information. The new edition will be thereby immensely useful to the students, practitioners and advanced readers. Key Features • Presents a considerably wide coverage of the field of embedded systems • Discusses the ARM microcontroller in detail • Provides numerous exercises to assess the learning process • Offers a good discussion on hardware–software codesign

Which came first, the system or the chip? While integrated circuits enable technology for the modern information age, computing, communication, and network chips fuel it. As soon as the integration ability of modern semiconductor technology offers presents opportunities, issues in power consumption, reliability, and form-factor present challenges. The demands of emerging software applications can only be met with unique systems and chips. Drawing on contributors from academia, research, and industry, Unique Systems and Chips explores unique approaches to designing future computing and communication chips and systems. The book focuses on specialized hardware and systems as opposed to general-purpose chips and systems. It covers early conception and simulation, mid-development, application, testing, and performance. The chapter authors introduce new ideas and innovations in unique aspects of chips and system design, then go on to provide in-depth analysis of these ideas. They explore ways in which these chips and systems may be used in further designs or products, spurring innovations beyond the intended scopes of those presented. International in flavor, the book brings industrial and academic perspectives into focus by presenting the full spectrum of applications of chips and systems.

Om hvordan mikroprocessorer fungerer, med undersøgelse af de nyeste mikroprocessorer fra Intel, IBM og Motorola.

Information in manual gives an overview of the ARM (Advanced RISC Machines) architecture. Describes the programmer's model, the ARM instruction set, the differences between 32-bit and 26-bit architectures, the Thumb instruction set, ARM system architecture, and the system control processer. Gives examples of coding algorithms.

Dynamically Reconfigurable Systems

Rapid System Prototyping with FPGAs

Optimizations and Exploration

The Definitive Guide to ARM® Cortex®-M3 and Cortex®-M4 Processors

Technology and Tools

The Definitive Guide to the ARM Cortex-M0

This title covers all software-related aspects of SoC design, from embedded and application-domain specific operating systems to system architecture for future SoC. It will give embedded software designers invaluable insights into the constraints imposed by the use of embedded software in an SoC context.

This book covers key concepts in the design of 2D and 3D Network-on-Chip interconnect. It highlights design challenges and discusses fundamentals of NoC technology, including architectures, algorithms and tools. Coverage focuses on topology exploration for both 2D and 3D NoCs, routing algorithms, NoC router design, NoC-based system integration, verification and testing, and NoC reliability. Case studies are used to illuminate new design methodologies.

The Arm(R) Cortex(R)-M processors are already one of the most popular choices for loT and embedded applications. With Arm Flexible Access and DesignStart(TM), accessing Arm Cortex-M processor IP is fast, affordable, and easy. This book introduces all the key topics that system-on-chip (SoC) and FPGA designers need to know when integrating a Cortex-M processor into their design, including bus protocols, bus interconnect, and peripheral designs. Joseph Yiu is a distinguished Arm engineer who began designing SoCs back in 2000 and has been a leader in this field for nearly twenty years. Joseph's book takes an expert look at what SoC designers need to know when incorporating Cortex-M processors into their systems. He discusses the on-chip bus protocol specifications (AMBA, AHB, and APB), used by Arm processors and a wide range of on-chip digital components such as memory interfaces, peripherals, and debug components. Software development and advanced design considerations are also covered. The journey concludes with 'Putting the system together', a designer's eye view of a simple microcontroller-like design based on the Cortex-M3 processor (DesignStart) that uses the components that you will have learned to create.

This book is about the Zynq-7000 All Programmable System on Chip, the family of devices from Xilinx that combines an application-grade ARM Cortex-A9 processor with traditional FPGA logic fabric. Catering for both new and experienced readers, it covers fundamental issues in an accessible way, starting with a clear overview of the device architecture, and an introduction to the design tools and processes for developing a Zynq SoC. Later chapters progress to more advanced topics such as embedded systems development, IP block design and operating systems. Maintaining a 'real-world' perspective, the book also compares Zynq with other device alternatives, and considers end-user applications. The Zynq Book is accompanied by a set of practical tutorials hosted on a companion website. These tutorials will guide the reader through first steps with Zynq, following on to a complete, audio-based embedded systems design.

Architectures, Design Methods and Applications

Co-verification of Hardware and Software for ARM SoC Design

With Pynq and Machine Learning Applications

Embedded Systems Design with Platform FPGAs

Memory Issues in Embedded Systems-on-Chip

The Quickest Path to Early Financial Independence

Memory Issues in Embedded Systems-On-Chip: Optimizations and Explorations is designed for different groups in the embedded systems-on-chip arena. First, it is designed for researchers and graduate students who wish to understand the research issues involved in memory system optimization and exploration for embedded systems-on-chip. Second, it is intended for designers of embedded systems who are migrating from a traditional micro-controllers centered, board-based design methodology to newer design methodologies using IP blocks for processor-core-based embedded systems-on-chip. Also, since Memory Issues in Embedded Systems-on-Chip: Optimization and Explorations illustrates a methodology for optimizing and exploring the memory configuration of embedded systems-on-chip, it is intended for managers and system designers who may be interested in the emerging capabilities of embedded systems-on-chip design methodologies for memory-intensive applications.

Until the late 1980s, information processing was associated with large mainframe computers and huge tape drives. During the 1990s, this trend shifted toward information processing with personal computers, or PCs. The trend toward miniaturization continues and in the future the majority of information processing systems will be small mobile computers, many of which will be embedded into larger products and interfaced to the physical environment. Hence, these kinds of systems are called embedded systems. Embedded systems together with their physical environment are called cyber-physical systems. Examples include systems such as transportation and fabrication equipment. It is expected that the total market volume of embedded systems will be significantly larger than that of traditional information processing systems such as PCs and mainframes. Embedded systems share a number of common characteristics. For example, they must be dependable, efficient, meet real-time constraints and require customized user interfaces (instead of generic keyboard and mouse interfaces). Therefore, it makes sense to consider common principles of embedded system design. Embedded System Design starts with an introduction into the area and a survey of specification models and languages for embedded and cyber-physical systems. It provides a brief overview of hardware devices used for such systems and presents the essentials of system software for embedded systems, like real-time operating systems. The book also discusses evaluation and validation techniques for embedded systems. Furthermore, the book presents an overview of techniques for mapping applications to execution platforms. Due to the importance of resource efficiency, the book also contains a selected set of optimization techniques for embedded systems, including special compilation techniques. The book closes with a brief survey on testing. Embedded System Design can be used as a text book for courses on embedded systems and as a source which provides pointers to relevant material in the area for PhD students and teachers. It assumes a basic knowledge of information processing hardware and software. Courseware related to this book is available at http://ls12-www.cs.tu-dortmund.de/~marwedel.

A PRACTICAL GUIDE TO HARDWARE FUNDAMENTALS Embedded Systems Hardware for Software Engineers describes the electrical and electronic circuits that are used in embedded systems, their functions, and how they can be interfaced to other devices. Basic computer architecture topics, memory, address decoding techniques, ROM, RAM, DRAM, DDR, cache memory, and memory hierarchy are discussed. The book covers key architectural features of widely used microcontrollers and microprocessors, including Microchip's PIC32, ATMEL's AVR32, and Freescale's MC68000. Interfacing to an embedded system is then described. Data acquisition system level design considerations and a design example are presented with real-world parameters and characteristics. Serial interfaces such as RS-232, RS-485, PC, and USB are addressed and printed circuit boards and high-speed signal propagation over transmission lines are covered with a minimum of math. A brief survey of logic families of integrated circuits and programmable logic devices is also contained in this in-depth resource. COVERAGE INCLUDES: Architecture examples Memory Memory address decoding Read-only memory and other related devices Input and output ports Analog-to-digital and digital-to-analog converters Interfacing to external devices Transmission lines Logic families of integrated circuits and their signaling characteristics The printed circuit board Programmable logic devices Test equipment: oscilloscopes and logic analyzers

mental improvements during the same period. What is clearly needed in verification techniques and technology is the equivalent of a synthesis productivity breakthrough. In the second edition of Writing Testbenches, Bergeron raises the verification level of abstraction by introducing coverage-driven constrained-random transaction-level self-checking testbenches all made possible through the introduction of hardware verification languages (HVLs), such as e from Verisity and OpenVera from Synopsys. The state-of-art methodologies described in Writing Test benches will contribute greatly to the much-needed equivalent of a synthesis breakthrough in verification productivity. I not only highly recommend this book, but also I think it should be required reading by anyone involved in design and verification of today's ASIC, SoCs and systems. Harry Foster Chief Architect Verplex Systems, Inc. xviii Writing Testbenches: Functional Verification of HDL Models PREFACE If you survey hardware design groups, you will learn that between 60% and 80% of their effort is now dedicated to verification.

Practical Examples in Verilog

For System-on-Chip Design

Embedded System Design

Reference Book
An Open-Source Research Platform for Heterogeneous Systems on Chip
Writing Testbenches: Functional Verification of HDL Models

This book provides a practical guide for engineers doing low power System-on-Chip (SoC) designs. It covers various aspects of low power design from architectural issues and design techniques to circuit design of power gating switches. In addition to providing a theoretical basis for these techniques, the book addresses the practical issues of implementing them in today's designs with today's tools.

Embedded Systems Design with Platform FPGAs introduces professional engineers and students alike to system development using Platform FPGAs. The focus is on embedded systems but it also serves as a general guide to building custom computing systems. The text describes the fundamental technology in terms of hardware, software, and a set of principles to guide the development of Platform FPGA systems. The goal is to show how to systematically and creatively apply these principles to the construction of application-specific embedded system architectures. There is a strong focus on using free and open source software to increase productivity. Each chapter is organized into two parts. The white pages describe concepts, principles, and general knowledge. The gray pages provide a technical rendition of the main issues of the chapter and show the concepts applied in practice. This includes step-by-step details for a specific development board and tool chain so that the reader can carry out the same steps on their own. Rather than try to demonstrate the concepts on a broad set of tools and boards, the text uses a single set of tools (Xilinx Platform Studio, Linux, and GNU) throughout and uses a single developer board (Xilinx ML-510) for the examples. Explains how to use the Platform FPGA to meet complex design requirements and improve product performance Presents both fundamental concepts together with pragmatic, step-by-step instructions for building a system on a Platform FPGA Includes detailed case studies, extended real-world examples, and lab exercises

The aim of this book is to provide a practical introduction to the foundations of modern operating systems, with a particular focus on GNU/Linux and the Arm platform. The unique perspective of the authors is that they explain operating systems theory and concepts but also ground them in practical use through illustrative examples.

An Open-Source Research Platform for Heterogeneous Systems on ChipBoD – Books on Demand
Acorn RISC Machine (ARM) Family Data Manual
Millionaire by Thirty
Embedded Processing with the Arm Cortex-A9 on the Xilinx Zynq-7000 All Programmable Soc
Advanced Chip Design
Networks on Chips
Best Practices in Design-for-prototyping