Cmos Test And Evaluation A Physical Perspective

This book treats important topics in "Acoustic Echo and Noise Control" and reports the latest developments. Methods for enhancing the quality of transmitted speech signals are gaining growing attention in universities and in industrial development laboratories. This book, written by an international team of highly qualified experts, concentrates on the modern and advanced methods.
CMOS Test and EvaluationA Physical PerspectiveSpringer
Lists citations with abstracts for aerospace related reports obtained from world wide sources and announces documents that have recently been entered into the NASA Scientific and Technical Information Database.
Scientific and Technical Aerospace Reports
Desk Reference
Power-Aware Testing and Test Strategies for Low Power Devices
CMOS Life Suitability Evaluation Program
Testing for Small-Delay Defects in Nanoscale CMOS Integrated Circuits

This book gives clear explanations of the technical aspects of electronics engineering from basic classical device formulations to the use of nanotechnology to develop efficient quantum electronic systems. As well as being up to date, this book provides a broader range of topics than found in many other electronics books. This book is written in a clear, accessible style and covers topics in a comprehensive manner. This book's approach is strongly application-based with key mathematical techniques introduced, helpful examples used to illustrate the design procedures, and case studies provided where appropriate. By including the fundamentals as well as more advanced techniques, the author has produced an up-to-date reference that meets the requirements of electronics and communications students and professional engineers. Features Discusses formulation and classification of integrated circuits Develops a hierarchical structure of functional logic blocks to build more complex digital logic circuits Outlines the structure of transistors (bipolar, JFET, MOSFET or MOS, CMOS), their processing techniques, their arrangement forming logic gates and digital circuits, optimal pass transistor stages of buffered chain, sources and types of noise, and performance of designed circuits under noisy conditions Explains data conversion processes, choice of the converter types, and inherent errors Describes electronic properties of nanomaterials, the crystallites' size reduction effect, and the principles of nanoscale structure fabrication Outlines the principles of quantum electronics leading to the development of lasers, masers, reversible quantum gates, and circuits and applications of quantum cells and fabrication methods, including self-assembly (quantum-dot cellular automata) and tunneling (superconducting circuits), and describes quantum error-correction techniques Problems are provided at the end of each chapter to challenge the reader's understanding

This thesis describes the design and implementation of a carry save adder cell for multivalued logic VLSI. A four valued system was chosen and the logic was analyzed and minimized using the HAMLET CAD tool. SPICE was used to design and simulate the required behavior of the current mode CMOS circuits. A VLSI test and evaluation integrated circuit was implemented with MAGIC and fabricated through the MOSIS service. The completed IC was tested and evaluated using a specially designed binary to multivalued logic converter and decoder. Engineering modifcations to the original current mode inverter cells used by HAMLET were made leading to significant power savings in a complete design. The fabricated device performed as predicted by SPICE simulation. Exhaustive functional testing produced correct steady-state output signals for all cases of input loadings. Finally, we show HAMLET minimization heuristics are not efficient in the design of adder cells by comparison with an alternative modulo 4 carry save adder cell in current mode CMOS.

Abstract: "A Test Chip has been designed and manufactured to evaluate different testing techniques for combinational or full-scan circuits. The Test Chip is a 25k gate CMOS gate-array using LSI Logic's LFT150K technology, and includes support (design-for-testability) circuitry and five types of circuits-under-test. Over 5,000 die have been manufactured. The five circuits-under-test include both data-path and synthesized control logic. The tests include design verification (simulation), exhaustive, pseudo-random, weighted random, and deterministic vectors for various fault models (stuck-at, transition, delay faults, and IDDQ testing). The chip will also be tested using the CrossCheck methodology, as well as other new techniques, including Stability Checking and Very-Low-Voltage Testing. The experiment includes an investigation of both serial and parallel signature analysis. This report describes the Test Evaluation Chip Experiment, including the design of the Test Chip and the tests applied. A future report will cover the experimental results and data analysis."

Process-Aware SRAM Design and Test
6th International Conference, NOLISP 2013, Mons, Belgium, June 19-21, 2013, Proceedings
Shortcomings in Ground Testing, Environment Simulations, and Performance Predictions for Space Applications
Publications of the National Bureau of Standards ... Catalog
Evaluation Engineering

The Electronic Device Failure Analysis Society proudly announces the Seventh Edition of the Microelectronics Failure Analysis Desk Reference, published by ASM International. The new edition will help engineers improve their ability to verify, isolate, uncover, and identify the root cause of failures. Prepared by a team of experts, this updated reference offers the latest information on advanced failure analysis tools and techniques, illustrated with numerous real-life examples. This book is geared to practicing engineers and for studies in the major area of power plant engineering. For non-metallurgists, a chapter has been devoted to the basics of material science, metallurgy of steels, heat treatment, and structure-property correlation. A chapter on materials for boiler tubes covers composition and application of different grades of steels and high temperature alloys currently in use as boiler tubes and future materials to be used in supercritical, ultra-supercritical and advanced ultra-supercritical thermal power plants. A comprehensive discussion on different mechanisms of boiler tube failure is the heart of the book. Additional chapters detailing the role of advanced material characterization techniques in failure investigation and the role of water chemistry in tube failures are key contributions to the book.

Device testing represents the single largest manufacturing expense in the semiconductor industry, costing over $40 billion a year. The most comprehensive and wide ranging book of its kind, Testing of Digital Systems covers everything you need to know about this vitally important subject. Starting right from the basics, the authors take the reader through automatic test pattern generation, design for testability and built-in self-test of digital circuits before moving on to more advanced topics such as IDDQ testing, functional testing, delay fault testing, memory testing, and fault diagnosis. The book includes detailed treatment of the latest techniques including test generation for various fault models, discussion of testing techniques at different levels of integrated circuit hierarchy and a chapter on system-on-a-chip test synthesis. Written for students and engineers, it is both an excellent senior/graduate level textbook and a valuable reference.

With the evolution of semiconductor technology and global diversification of the semiconductor business, testing of semiconductor devices to systems for electrostatic discharge (ESD) and electrical overstress (EOS) has increased in importance. ESD Testing: From Components to Systems updates the reader in the new tests, test models, and techniques in the characterization of semiconductor components for ESD, EOS, and latchup. Key features: Provides understanding and knowledge of ESD models and specifications including human body model (HBM), machine model (MM), charged device model (CDM), charged board model (CBM), cable discharge events (CDE), human metal model (HMM), IEC 61000-4-2 and IEC 61000-4-5. Discusses new testing methodologies such as transmission line pulse (TLP), to very fast transmission line pulse (VF-TLP), and future methods of long pulse TLP, to ultra-fast TLP (UF-TLP). Describes both conventional testing and new testing techniques for both chip and system level evaluation. Addresses EOS testing, electromagnetic compatibility (EMC) scanning, to current reconstruction methods. Discusses latchup characterization and testing methodologies for evaluation of semiconductor technology to product testing. ESD Testing: From Components to Systems is part of the authors' series of books on electrostatic discharge (ESD) protection; this book will be an invaluable reference for the professional semiconductor chip and system-level ESD and EOS test engineer. Semiconductor device and process development, circuit designers, quality, reliability and failure analysis engineers will also find it an essential reference. In addition, its academic treatment will appeal to both senior and graduate students with interests in semiconductor process, device physics, semiconductor testing and experimental work.

Electronics
An Experimental Chip to Evaluate Test Techniques
Source Modeling Techniques for Quality Enhancement in Statistical Parametric Speech Synthesis
Microelectronic Test Structures for CMOS Technology
From Components to Systems

The monograph will be dedicated to SRAM (memory) design and test issues in nano-scaled technologies by adapting the cell design and chip design considerations to the growing process variations with associated test issues. Purpose: provide process-aware solutions for SRAM design and test challenges.
CMOS Test and Evaluation: A Physical Perspective is a single source for an integrated view of test and data analysis methodology for CMOS products, covering circuit sensitivities to MOSFET characteristics, impact of silicon technology process variability, applications of embedded test structures and sensors, product yield, and reliability over the lifetime of the product. This book also covers statistical data analysis and visualization techniq test equipment and CMOS product specifications, and examines product behavior over its full voltage, temperature and frequency range.
Managing the power consumption of circuits and systems is now considered one of the most important challenges for the semiconductor industry. Elaborate power management strategies, such as dynamic voltage scaling, clock gating or power gating techniques, are used today to control the power dissipation during functional operation. The usage of these strategies has various implications on manufacturing test, and power-aware test is therefore increasingly becoming a major consideration during design-for-test and test preparation for low power devices. This book explores existing solutions for power-aware test and design-for-test of conventional circuits and systems, and surveys test strategies and EDA solutions for testing low power devices.
Annual Report, March 1 to November 1, 1978
IDDQ Testing of VLSI Circuits
Technical Abstract Bulletin
Microcircuit Reliability Bibliography
CMOS Test and Evaluation
Includes bibliographical references and index.
This book provides a new multi-method, process-oriented approach towards speech quality assessment, which allows readers to examine the influence of speech transmission quality on a variety of perceptual and cognitive processes in human listeners. Fundamental concepts and methodologies surrounding the topic of process-oriented quality assessment are introduced and discussed. The book further describes a functional process model of human quality perception, which theoretically integrates results obtained in three experimental studies. This book's conceptual ideas, empirical findings, and theoretical interpretations should be of particular interest to researchers working in the fields of Quality and Usability Engineering, Audio Engineering, Psychoacoustics, Audiology, and Psychophysiology.
This book presents a statistical parametric speech synthesis (SPSS) framework for developing a speech synthesis system where the desired speech is generated from the parameters of vocal tract and excitation source. Throughout the book, the authors discuss novel source modeling techniques to enhance the naturalness and overall intelligibility of the SPSS system. This book provides several important methods and models for generating the excitation source parameters for enhancing the overall quality of synthesized speech. The contents of the book are useful for both researchers and system developers. For researchers, the book is useful for knowing the current state-of-the-art excitation source models for SPSS and further refining the source models to incorporate the realistic semantics present in the text. For system developers, the book is useful to integrate the sophisticated excitation source models mentioned to the latest models of mobile/smart phones.
Cargo Movement Operations System (CMOS) Software Test Plan. Final
Human Information Processing in Speech Quality Assessment
NASA Technical Paper
Haas, Elsa (singer)
ESD Testing
The objective of this work was to determine baseline electrical parameters that could be used to evaluate a fabrication process. Two lots of wafers containing NBS-16 test chips were fabricated at a commercial vendor in a radiation-hard, CMOS/SOS process. These wafers were then returned to NBS for testing and evaluation. Testing was performed using an automated computer-controlled integrated circuit test system. Test results were evaluated using analysis techniques which provided a statistical estimate of selected parameters and identified spatial correlations between data sets. Further analysis was then performed in order to identify process irregularities. A complete description of the test results and analysis procedure can be found in the appendices.
The results of a matrix of high-temperature accelerated life tests, 125C life tests, and 250 hour 250C lot acceptance tests were evaluated to determine the reliabiltiy of a cross-section of the complementary metal oxide semiconductor (CMOS) family of devices. The devices evaluated included a NOR gate, a flip-flop, a four bit adder, and a counter/divider. Each device was procured from two different manufacturers, and from three different lots of each manufacturer. The correlation of the Lot Acceptance data with the reliability of the devices revealed that the Class S Lot Acceptance Test, as specified in MIL-STD-883, Method 500.5 is approximately 50% effective screening for lot reliability. To minimize the possibility of rejecting good lots and/or accepting bad lots, two temperature Lot Acceptance Test is recommended. Using a two temperature Lot Acceptance Test at temperature above 200 C would permit control of both the activation energy and pre-exponential factor in the Arrhenius model. A 100% burn-9n is also recommended. Although burn-in would not improve all lots, it would improve the reliability of those lots which have a freak population with a high failure rate.
The purpose of this Technical Report is to review the Software Test Plan, Final, CDRL A007-03, which was produced for the Government by Evaluation Research Corporation. The results are provided in the form of Data Item Discrepancy worksheets as requested by the CMOS Program Office.
Part 1
Proceedings of the ... IEEE International Conference on Microelectronic Test Structures
A CMOS Current-mode Full-adder Cell for Multi-valued Logic VLSI
Test Generation and Evaluation for Bridging Faults in CMOS VLSI Circuits
Evaluation of a CMOS/SOS Process Using Process Validation Wafers
Transient current (iDDT) refers to the current drawn from the power supply durin g the transient switching of CMOS gates. Testing based on the transient current can detect many of the defects that can occur in ICs, such as resistive opens, w hich may not be detected by traditional voltage testing or by Leakage current (I DDQ) testing methods. A major set back for IDDQ testing methods is the increased leakage currents in today's ICs. Thus iDDT based testing has been often investi gated as an alternative or supplement to (IDDQ) testing. Little work has focused on iDDT testing for domino circuits. In this thesis, we propose a method for testing domino CMOS circuits using the transient power supp ly current. The method is based on monitoring the peak value of the transient cu rrent. This peak varies considerably with process variations, so each process ha s different thresholds; this problem will be addressed by proposing a normalizat ion procedure that allows us to use a single threshold for all processes. We pre sent also a test vector generation algorithm for testing large domino circuits. We evaluate the effectiveness of this testing method by simulation on various do mino circuits of different sizes. We develop and implement a partitioning technique to improve the fault coverage of the test method when used with large circuits. The algorithm divides the circ uit into different clusters where each cluster is fed by a different power suppl y branch. We also provide an automation system to simplify the process of genera ting the simulation files, injecting the defects in the circuit, running the sim ulations, storing the simulations output, processing the output signals, and fin ally gathering and analyzing the results.
An efficient automatic test pattern generator for I$sb{DDQ}$ current testing of CMOS digital circuits is presented. The complete two-line bridging fault set is considered. Because of the time constraints of I$sb{DDQ}$ testing, an adaptive genetic algorithm (GA) is used to generate compact test sets. To accurately evaluate the test sets, fault grading is performed using a switch-level fault simulator and a mixed-mode electrical-level fault simulator. The test sets are compared with those generated by HITEC, a traditional gate-level test generator. Experimental results for ISCAS85 and ISCAS89 benchmark circuits are presented. The results show that for I$sb{DDQ}$ testing, the GA test sets outperform the HITEC test sets. When the test sets are truncated due to test time constraints, the fault coverages can differ by 10% or more. In addition to test generation and test evaluation, diagnosis (fault location) is also performed using both test sets. Diagnosis is performed using fault dictionaries constructed during test evaluation. In addition to the traditional full dictionary, two reduced dictionaries are also presented. The results show that the reduced dictionaries offer good size-resolution trade-offs when compared with the full dictionary.
Advances in design methods and process technologies have resulted in a continuous increase in the complexity of integrated circuits (ICs). However, the increased complexity and nanometer-size features of modern ICs make them susceptible to manufacturing defects, as well as performance and quality issues. Testing for Small-Delay Defects in Nanoscale CMOS Integrated Circuits covers common problems in areas such as process variations, power supply noise, crosstalk, resistive opens/bridges, and design-for-manufacturing (DfM)-related rule violations. The book also addresses testing for small-delay defects (SDDs), which can cause immediate timing failures on both critical and non-critical paths in the circuit. Overviews semiconductor industry test challenges and the need for SDD testing, including basic concepts and introductory material Describes algorithmic solutions incorporated in commercial tools from Mentor Graphics Reviews SDD testing based on "alternative methods" that explores new metrics, top-off ATPG, and circuit topology-based solutions Highlights the advantages and disadvantages of a diverse set of metrics, and identifies scope for improvement Written from the triple viewpoint of university researchers, EDA tool developers, and chip designers and tool users, this book is the first of its kind to address all aspects of SDD testing from such a diverse perspective. The book is designed as a one-stop reference for current industrial practices, research challenges in the domain of SDD testing, and recent developments in SDD solutions.
CMOS SRAM Circuit Design and Parametric Test in Nano-Scaled Technologies
Gamma Irradiation Testing of Electronic Devices, and Evaluation of Irradiated CMOS Components on MOSIS Test Chips
A Process Development and Quality Evaluation Test Chip for Double-level Metal CMOS
from Classical to Quantum
A CMOS Current-Mode Full-Adder Cell for Multi-Valued Logic VLSI.

Microelectronic Test Structures for CMOS Technology and Products addresses the basic concepts of the design of test structures for incorporation within test-vehicles, scribe-lines, and CMOS products. The role of test structures in the development and monitoring of CMOS technologies and products has become ever more important with the increased cost and complexity of development and manufacturing. In this timely volume, IBM scientists Manjul Bhushan and Mark Ketchen emphasize high speed characterization techniques for digital CMOS circuit applications and bridging between circuit performance and characteristics of MOSFETs and other circuit elements. Detailed examples are presented throughout, many of which are equally applicable to other microelectronic technologies as well. The authors' overarching goal is to provide students and technology practitioners alike a practical guide to the disciplined design and use of test structures that give unambiguous information on the parametrics and performance of digital CMOS technology.
Material in the Australian performing arts programs and ephemera (PROMPT) collection consists of programs and related items for Australian performing arts organisations, Australian artists performing overseas, professional productions performed in Australia (including those featuring overseas performers) and overseas performances of Australian plays, music, etc.
This book constitutes the proceedings of the 6th International Conference on Nonlinear Speech Processing, NOLISP 2013, held in Mons, Belgium, in June 2013. The 27 refereed papers included in this volume were carefully reviewed and selected from 34 submissions. The paper are organized in topical sections on speech and audio analysis; speech synthesis; speech-based biomedical applications; automatic speech recognition; and speech enhancement.
Programs and Related Material Collected by the National Library of Australia].

Microelectronics Failure Analysis
Evaluation of Dynamic Current Testing for CMOS Domino Circuits
A Physical Perspective

Power supply current monitoring to detect CMOS IC defects during production testing quietly laid down its roots in the mid-1970s. Both Sandia Labs and RCA in the United States and Philips Labs in the Netherlands practiced this procedure on their CMOS ICs. At that time, this practice stemmed simply from an intuitive sense that CMOS ICs showing abnormal quiescent power supply current (IDDQ) contained defects. Later, this intuition was supported by data and analysis in the 1980s by Levi (RACD, Malaiya and Su (SUNY-Binghamton), Soden and Hawkins (Sandia Labs and the University of New Mexico), Jacomino and co-workers (Laboratoire d'Automatique de Grenoble), and Maly and co-workers (Carnegie Mellon University). Interest in IDDQ testing has advanced beyond the data reported in the 1980s and is now focused on applications and evaluations involving larger volumes of ICs that improve quality beyond what can be achieved by previous conventional means. In the conventional style of testing one attempts to propagate the logic states of the suspended nodes to primary outputs. This is done for all or most nodes of the circuit. For sequential circuits, in particular, the complexity of finding suitable tests is very high. In comparison, the IDDQ test does not observe the logic states, but measures the integrated current that leaks through all gates. In other words, it is like measuring a patient's temperature to determine the state of health. Despite perceived advantages, during the years that followed its initial announcements, skepticism about the practicality of IDDQ testing prevailed. The idea, however, provided a great opportunity to researchers. New results on test generation, fault simulation, design for testability, built-in self-test, and diagnosis for this style of testing have since been reported. After a decade of research, we are definitely closer to practice.
Proceedings of the ... IEEE International Conference on Microelectronic Test Structures, ICMTS.
Topics in Acoustic Echo and Noise Control
Journal of Research of the National Bureau of Standards
NBS Special Publication
Testing of Digital Systems