Introduction To Logic Synthesis Using Verilog Hdl

Introduction to Logic Synthesis Using Verilog HDL explains how to write accurate Verilog descriptions of digital systems that can be synthesized into digital system netlists with desirable characteristics. The book contains numerous Verilog examples that begin with simple combinational networks and progress to synchronous sequential logic systems. Common pitfalls in the development of synthesizable Verilog HDL are also discussed along with methods for avoiding them. The target audience is anyone with a basic understanding of digital logic principles who wishes to learn how to model digital systems in the Verilog HDL in a manner that also allows for automatic synthesis. A wide range of readers, from hobbyists and undergraduate students to seasoned professionals, will find this a compelling and approachable work. The book provides concise coverage of the material and includes many examples, enabling readers to quickly generate high-quality synthesizable Verilog models.

VERILOG HDL, Second Editionby Samir PalnitkarWith a Foreword by Prabhu GoelWritten forboth experienced and new users, this book gives you broad coverage of VerilogHDL. The book stresses the practical design and verification perspective ofVerilog rather than emphasizing only the language aspects. The informationpresented is fully compliant with the IEEE 1364-2001 Verilog HDL standard. Among its many features, this edition- bull; bull;Describes state-of-the-art verification methodologies bull;Provides full coverage of gate, dataflow (RTL), behavioral and switch modeling bull;Introduces you to the Programming Language Interface (PLI) bull;Describes logic synthesis methodologies bull;Explains timing and delay simulation bull;Discusses user-defined primitives bull;Offers many practical modeling tips Includes over 300 illustrations, examples, and exercises, and a Verilog resource list.Learning objectives and summaries are provided for each chapter. About the CD-ROMThe CD-ROM contains a Verilog simulator with agraphical user interface and the source code for the examples in the book. Whatpeople are saying about Verilog HDL- "Mr.Palnitkar illustrates how and why Verilog HDL is used to develop today'smost complex digital designs. This book is valuable to both the novice and theexperienced Verilog user. I highly recommend it to anyone exploring Verilogbased design." -RajeevMadhavan, Chairman and CEO, Magma Design Automation "Thisbook is unique in its breadth of information on Verilog and Verilog-relatedtopics. It is fully compliant with the IEEE 1364-2001 standard, contains allthe information that you need on the basics, and devotes several chapters toadvanced topics such as verification, PLI, synthesis and modelingtechniques." -MichaelMcNamara, Chair, IEEE 1364-2001 Verilog Standards Organization Thishas been my favorite Verilog book since I picked it up in college. It is theonly book that covers practical Verilog. A must have for beginners andexperts." -BerendOzceri, Design Engineer, Cisco Systems, Inc. "Simple,logical and well-organized material with plenty of illustrations, makes this anideal textbook." -Arun K. Somani, Jerry R. Junkins Chair Professor,Department of Electrical and Computer Engineering, Iowa State University, Ames PRENTICE HALL Professional Technical Reference Upper Saddle River, NJ 07458 www.phptr.com ISBN: 0-13-044911-3

Designing Asynchronous Circuits using NULL Convention Logic (NCL) begins with an introduction to asynchronous (clockless) logic in general, and then focuses on delay-insensitive asynchronous logic design using the NCL paradigm. The book details design of input-complete and observable dual-rail and quad-rail combinational circuits, and then discusses implementation of sequential circuits, which require datapath feedback. Next, throughput optimization techniques are presented, including pipelining, embedding registration, early completion, and NULL cycle reduction. Subsequently, low-power design techniques, such as wavefront steering and Multi-Threshold CMOS (MTCMOS) for NCL, are discussed. The book culminates with a comprehensive design example of an optimized Greatest Common Divisor circuit. Readers should have prior knowledge of basic logic design concepts, such as Boolean algebra and Karnaugh maps. After studying this book, readers should have a good understanding of the differences between asynchronous and synchronous circuits, and should be able to design arbitrary NCL circuits, optimized for area, throughput, and power. Table of Contents: Introduction to Asynchronous Logic / Overview of NULL Convention Logic (NCL) / Combinational NCL Circuit Design / Sequential NCL Circuit Design / NCL Throughput Optimization / Low-Power NCL Design / Comprehensive NCL Design Example

For the first time in book form, this comprehensive and systematic monograph presents methods for the reversible synthesis of logic functions and circuits. It is illustrated with a wealth of examples and figures that describe in detail the systematic methodologies of synthesis using reversible logic.

Designing Asynchronous Circuits Using NULL Convention Logic (NCL)

An Introduction to Logic Circuit Testing

Logic Synthesis Using Synopsys®

VHDL for Logic Synthesis

Introduction to Digital Systems

This is the first volume in a new hardcover combined volume of Synthesis Lectures. This volume contains the following lectures: Finite State Machine Datapath Design, Optimization, and Implementation; Introduction to Logic Synthesis using Verilog HDL; High-Speed Digital System Design; Microcontrollers Fundamentals for Engineers and Scientists

Finite State Machine Datapath Design, Optimization, and Implementation explores the design space of combined FSM/Datapath implementations. The lecture starts by examining performance issues in digital systems such as clock skew and its effect on setup and hold time constraints, and the use of pipelining for increasing system clock frequency. This is followed by definitions for latency and throughput, with associated resource tradeoffs explored in detail through the use of dataflow graphs and scheduling tables applied to examples taken from digital signal processing applications. Also, design issues relating to functionality, interfacing, and performance for different types of memories commonly found in ASICs and FPGAs such as FIFOs, single-ports, and dual-ports are examined. Selected design examples are presented in implementation-neutral Verilog code and block diagrams, with associated design files available as downloads for both Altera Quartus and Xilinx Virtex FPGA platforms. A working knowledge of Verilog, logic synthesis, and basic digital design techniques is required. This lecture is suitable as a companion to the synthesis lecture titled Introduction to Logic Synthesis using Verilog HDL. Table of Contents: Calculating Maximum Clock Frequency / Improving Design Performance / Finite State Machine with Datapath (FSMD) Design / Embedded Memory Usage in Finite State Machine with Datapath (FSMD) Designs

XV From the Old to the New xvii Acknowledgments xx| Verilog A Tutorial Introduction Getting Started 2 A Structural Description 2 Simulating the binaryToESeg Driver 4 Creating Ports For the Module 7 Creating a Testbench For a Module 8 Behavioral Modeling of Combinational Circuits 11 Procedural Models 12 Rules for Synthesizing Combinational Circuits 13 Procedural Modeling of Clocked Sequential Circuits 14 Modeling Finite State Machines 15 Rules for Synthesizing Sequential Systems 18 Non-Blocking Assignment ("

Pragmatic Logic presents the analysis and design of digital logic systems. The author begins with a brief study of binary and hexadecimal number systems and then looks at the basics of Boolean algebra. The study of logic circuits is divided into two parts, combinational logic, which has no memory, and sequential logic, which does. Numerous examples highlight the principles being presented. The text ends with an introduction to digital logic design using Verilog, a hardware description language. The chapter on Verilog can be studied along with the other chapters in the text. After the reader has completed combinational logic in Chapters 4 and 5, sections 9.1 and 9.2 would be appropriate. Similarly, the rest of Chapter 9 could be studied after completing sequential logic in Chapters 6 and 7. This short lecture book will be of use to students at any level of electrical or computer engineering and for practicing engineers or scientists in any field looking for a practical and applied introduction to digital logic. The author's "pragmatic" and applied style gives a unique and helpful "non-idealist, practical, opinionated" introduction to digital systems.

With an Introduction to Verilog and FPGA-Based Design

Logic Synthesis and Verification Algorithms

Logic Synthesis for Low Power VLSI Designs

Verilog Coding for Logic Synthesis

Modeling, Synthesis, and Simulation Using VHDL

This book is a gentle but rigorous introduction to formal logic. It is intended primarily for use at the college level. However, it can also be used for advanced secondary school students, and it can be used at the start of graduate school for those who have not yet seen the material. The approach to teaching logic used here emerged from more than 20 years of teaching logic to students at Stanford University and from teaching logic to tens of thousands of others via online courses on the World Wide Web. The approach differs from that taken by other books in logic in two essential ways, one having to do with content, the other with form. Like many other books on logic, this one covers logical syntax and semantics and proof theory plus induction. However, unlike other books, this book begins with Herbrand semantics rather than the more traditional Tarskian semantics. This approach makes the material considerably easier for students to understand and leaves them with a deeper understanding of what logic is all about. The primary content difference concerns the semantics of the logic that is taught. In addition to this text, there are online exercises (with automated grading), online logic tools and applications, online videos of lectures, and an online forum for discussion. They are available at logic.stanford.edu/intrologic/.

Research and development of logic synthesis and verification have matured considerably over the past two decades. Many commercial products are available, and they have been critical in harnessing advances in fabrication technology to produce today's plethora of electronic components. While this maturity is assuring, the advances in fabrication continue to seemingly present unwieldy challenges. Logic Synthesis and Verification provides a state-of-the-art view of logic synthesis and verification. It consists of fifteen chapters, each focusing on a distinct aspect. Each chapter presents key developments, outlines future challenges, and lists essential references. Two unique features of this book are technical strength and comprehensiveness. The book chapters are written by twenty-eight recognized leaders in the field and reviewed by equally qualified experts. The topics collectively span the field. Logic Synthesis and Verification fills a current gap in the existing CAD literature. Each chapter contains essential information to study a topic at a great depth, and to understand further developments in the field. The book is intended for seniors, graduate students, researchers, and developers of related Computer-Aided Design (CAD) tools. From the foreword: "The commercial success of logic synthesis and verification is due in large part to the ideas of many of the authors of this book. Their innovative work contributed to design automation tools that permanently changed the course of electronic design." by Aart J. de Geus, Chairman and CEO, Synopsys, Inc.

Short turnaround has become critical in the design of electronic systems. Software- programmable components such as microprocessors and digital signal processors have been used extensively in such systems since they allow rapid design revisions. However, the inherent performance limitations of software-programmable systems mean that they are inadequate for high-performance designs. Designers thus turned to gate arrays as a solution. User-programmable gate arrays (field-programmable gate arrays, FPGAs) have recently emerged and are changing the way electronic systems are designed and implemented. The growing complexity of the logic circuits that can be packed onto an FPGA chip means that it has become important to have automatic synthesis tools that implement logic functions on these architectures. Logic Synthesis for Field-Programmable Gate Arrays describes logic synthesis for both look-up table (LUT) and multiplexor-based architectures, with a balanced presentation of existing techniques together with algorithms and the system developed by the authors. Audience: A useful reference for VLSI designers, developers of computer-aided design tools, and anyone involved in or with FPGAs.

Introduction to Logic Synthesis Using Verilog HDLMorgan & Claypool Publishers

Digital Logic Design Using Verilog

Digital Logic

Sequential Logic

Switching Theory for Logic Synthesis

Introduction to Logic Circuits & Logic Design with Verilog

This book describes the synthesis of logic functions using memories. It is useful to design field programmable gate arrays (FPGAs) that contain both small-scale memories, called look-up tables (LUTs), and medium-scale memories, called embedded memories. This is a valuable reference for both FPGA system designers and CAD tool developers, concerned with logic synthesis for FPGAs.

This text is intended as an introduction to mathematical proofs for students. It is distilled from the lecture notes for a course focused on set theory subject matter as a means of teaching proofs. Chapter 1 contains an introduction and provides a brief summary of some background material students may be unfamiliar with. Chapters 2 and 3 introduce the basics of logic for students not yet familiar with these topics. Included is material on Boolean logic, propositions and predicates, logical operations, truth tables, tautologies and contradictions, rules of inference and logical arguments. Chapter 4 introduces mathematical proofs, including proof conventions, direct proofs, proof-by-contradiction, and proof-by-contraposition. Chapter 5 introduces the basics of naive set theory, including Venn diagrams and operations on sets. Chapter 6 introduces mathematical induction and recurrence relations. Chapter 7 introduces set-theoretic functions and covers injective, surjective, and bijective functions, as well as permutations. Chapter 8 covers the fundamental properties of the integers including primes, unique factorization, and Euclid's algorithm. Chapter 9 is an introduction to combinatorics; topics included are combinatorial proofs, binomial and multinomial coefficients, the Inclusion-Exclusion principle, and counting the number of surjective functions between finite sets. Chapter 10 introduces relations and covers equivalence relations and partial orders. Chapter 11 covers number bases, number systems, and operations. Chapter 12 covers cardinality, including basic results on countable and uncountable infinities, and introduces cardinal numbers. Chapter 13 expands on partial orders and introduces ordinal numbers. Chapter 14 examines the paradoxes of naive set theory and introduces and discusses axiomatic set theory. This chapter also includes Cantor's Paradox, Russel's Paradox, a discussion of axiomatic theories, an exposition on Zermelo-Fraenkel Set Theory with the Axiom of Choice, and a brief explanation of Gödel's Incompleteness Theorems.

The roots of the project which culminates with the writing of this book can be traced to the work on logic synthesis started in 1979 at the IBM Watson Research Center and at University of California, Berkeley. During the preliminary phases of these projects, the impor tance of logic minimization for the synthesis of area and performance effective circuits clearly emerged. In 1980, Richard Newton stirred our interest by pointing out new heuristic algorithms for two-level logic minimization and the potential for improving upon existing approaches. In the summer of 1981, the authors organized and participated in a seminar on logic manipulation at IBM Research. One of the goals of the seminar was to study the literature on logic minimization and to look at heuristic algorithms from a fundamental and comparative point of view. The fruits of this investigation were surprisingly abundant: it was apparent from an initial implementation of recursive logic minimiza tion (ESPRESSO-I) that, if we merged our new results into a two-level minimization program, an important step forward in automatic logic synthesis could result. ESPRESSO-II was born and an APL implemen tation was created in the summer of 1982. The results of preliminary tests on a fairly large set of industrial examples were good enough to justify the publication of our algorithms. It is hoped that the strength and speed of our minimizer warrant its Italian name, which denotes both express delivery and a specially-brewed black coffee.

This book is a gentle but rigorous introduction to Formal Logic. It is intended primarily for use at the college level. However, it can also be used for advanced secondary school students, and it can be used at the start of graduate school for those who have not yet seen the material. The approach to teaching logic used here emerged from more than 20 years of teaching logic to students at Stanford University and from teaching logic to tens of thousands of others via online courses on the World Wide Web. The approach differs from that taken by other books in logic in two essential ways, one having to do with content, the other with form. Like many other books on logic, this one covers logical syntax and semantics and proof theory plus induction. However, unlike other books, this book begins with Herbrand semantics rather than the more traditional Tarskian semantics. This approach makes the material considerably easier for students to understand and leaves them with a deeper understanding of what logic is all about. In addition to this text, there are online exercises (with automated grading), online logic tools and applications, online videos of lectures, and an online forum for discussion. They are available at logic.stanford.edu/intrologic/ Table of Contents: Introduction / Propositional Logic / Satisfiability / Propositional Proofs / Propositional Resolution / Relational Logic / Relational Logic Proofs / Resolution / Induction / Equality

Introduction to Logic Synthesis using Verilog HDL

Memory-Based Logic Synthesis

New Data Structures and Algorithms for Logic Synthesis and Verification

The Verilog® Hardware Description Language

Advanced Techniques in Logic Synthesis, Optimizations and Applications

This book provides the most up-to-date coverage using the Synopsys program in the design of integrated circuits. The incorporation of "synthesis tools" is the most popular new method of designing integrated circuits for higher speeds covering smaller surface areas. Synopsys is the dominant computer-aided circuit design program in the world. All of the major circuit manufacturers and ASIC design firms use Synopsys. In addition, Synopsys is used in teaching and laboratories at over 600 universities. First practical guide to using synthesis with Synopsys Synopsys is the #1 design program for IC design

Logic Synthesis for Low Power VLSI Designs presents a systematic and comprehensive treatment of power modeling and optimization at the logic level. More precisely, this book provides a detailed presentation of methodologies, algorithms and CAD tools for power modeling, estimation and analysis, synthesis and optimization at the logic level. Logic Synthesis for Low Power VLSI Designs contains detailed descriptions of technology-dependent logic transformations and optimizations, technology decomposition and mapping, and post-mapping structural optimization techniques for low power. It also emphasizes the trade-off techniques for two-level and multi-level logic circuits that involve power dissipation and circuit speed, in the hope that the readers can better understand the issues and ways of achieving their power dissipation goal while meeting the timing constraints. Logic Synthesis for Low Power VLSI Designs is written for VLSI design engineers, CAD professionals, and students who have had a basic knowledge of CMOS digital design and logic synthesis.

A unique guide to using both modeling and simulation in digital systems design Digital systems design requires rigorous modeling and simulation analysis that eliminates design risks and potential harm to users. Introduction to Digital Systems: Modeling, Synthesis, and Simulation Using VHDL introduces the application of modeling and synthesis in the effective design of digital systems and explains applicable analytical and computational methods. Through step-by-step explanations and numerous examples, the author equips readers with the tools needed to model, synthesize, and simulate digital principles using Very High Speed Integrated Circuit Hardware Description Language (VHDL) programming. Extensively classroom-tested to ensure a fluid presentation, this book provides a comprehensive overview of the topic by integrating theoretical principles, discrete mathematical models, computer simulations, and basic methods of analysis. Topical coverage includes: Digital systems modeling and simulation Integrated logic Boolean algebra and logic Logic function optimization Number systems Combinational logic VHDL design concepts Sequential and synchronous sequential logic Each chapter begins with learning objectives that outline key concepts that follow, and all discussions conclude with problem sets that allow readers to test their

comprehension of the presented material. Throughout the book, VHDL sample codes are used to illustrate circuit design, providing guidance not only on how to learn and master VHDL programming, but also how to model and simulate digital circuits. Introduction to Digital Systems is an excellent book for courses in modeling and simulation, operations research, engineering, and computer science at the upper-undergraduate and graduate levels. The book also serves as a valuable resource for researchers and practitioners in the fields of operations research, mathematical modeling, simulation, electrical engineering, and computer science.

Until now, there was no single resource for actual digital system design. Using both basic and advanced concepts, Sequential Logic: Analysis and Synthesis offers a thorough exposition of the analysis and synthesis of both synchronous and asynchronous sequential machines. With 25 years of experience in designing computing equipment, the author stresses the practical design of state machines. He clearly delineates each step of the structured and rigorous design principles that can be applied to practical applications. The book begins by reviewing the analysis of combinatorial logic and Boolean algebra, and goes on to define sequential machines and discuss traditional and alternative methods for synthesizing synchronous sequential machines. The final chapters deal with asynchronous sequential machines and pulse-mode asynchronous sequential machines. Because this volume is technology-independent, these techniques can be used in a variety of fields, such as electrical and computer engineering as well as nanotechnology. By presenting each method in detail, expounding on several corresponding examples, and providing over 500 useful figures, Sequential Logic is an excellent tutorial on analysis and synthesis procedures.

Introduction to Logic

An Introduction to Proofs with Set Theory

Logic Synthesis and Optimization

Pragmatic Logic

Making VHDL a simple and easy-to-use hardware description language Many engineers encountering VHDL (very high speed integrated circuits hardware description language) for the first time can feel overwhelmed by it. This book bridges the gap between the VHDL language and the hardware that results from logic synthesis with clear organisation, progressing from the basics of combinational logic, types, and operators; through special structures such as tristate buses, register banks and memories, to advanced themes such as developing your own packages, writing test benches and using the full range of synthesis types. This third edition has been substantially rewritten to include the new VHDL-2008 features that enable synthesis of fixed-point and floating-point hardware. Extensively updated throughout to reflect modern logic synthesis usage, it also contains a complete case study to demonstrate the updated features. Features to this edition include: a common VHDL subset which will work across a range of different synthesis systems, targeting a very wide range of technologies a design style that results in long design lifetimes, maximum design reuse and easy technology retargeting a new chapter on a large scale design example based on a digital filter from design objective and design process, to testing strategy and test benches a chapter on writing test benches, with everything needed to implement a test-based design strategy extensive coverage of data path design, including integer, fixed-point and floating-point arithmetic, logic circuits, shifters, tristate buses, RAMs, ROMs, state machines, and decoders Focused specifically on logic synthesis, this book is for professional hardware engineers using VHDL for logic synthesis, and digital systems designers new to VHDL but familiar with digital systems. It offers all the knowledge and tools needed to use VHDL for logic synthesis. Organised in themed chapters and with a comprehensive index, this complete reference will also benefit postgraduate students following courses on microelectronics or VLSI/ semiconductors and digital design.

Finite State Machine-Datapath Design, Optimization, and Implementation explores the design space of combined FSM/Datapath implementations. The lecture starts by examining performance issues in digital systems such as clock skew and its effect on setup and hold time constraints, and the use of pipelining for increasing system clock frequency. This is followed by definitions for latency and throughput, with associated resource tradeoffs explored in detail through the use of dataflow graphs and scheduling tables applied to examples taken from digital signal processing applications. Also, design issues relating to functionality, interfacing, and performance for different types of memories commonly found in ASICs and FPGAs such as FIFOs, single-ports, dual-ports, and register files are examined. Finally, design issues regarding cooperating Finite State Machine/Datapaths are explored. All design examples are presented in implementation-neutral Verilog code and block diagrams, with associated design files available as downloads for both Altera Quartus and Xilinx Virtex FPGA platforms. A working knowledge of Verilog, logic synthesis, and basic digital design techniques is required. This lecture is suitable as a companion to the synthesis lecture titled Introduction to Logic Synthesis using Verilog HDL.

Pragmatic Logic presents the analysis and design of digital logic systems. The author begins with a brief study of binary and hexadecimal number systems and then looks at the basics of Boolean algebra. The study of logic circuits is divided into two parts, combinational logic, which has no memory, and sequential logic, which does. Numerous examples highlight the principles being presented. The text ends with an introduction to digital logic design using Verilog, a hardware description language. The chapter on Verilog can be studied along with the other chapters in the text. After the reader has completed combinational logic in Chapters 4 and 5, sections 9.1 and 9.2 would be appropriate. Similarly, the rest of Chapter 9 could be studied after completing sequential logic in Chapters 6 and 7. This short lecture book will be of use to students at any level of electrical or computer engineering and for practicing engineers or scientists in any field looking for a practical and applied introduction to digital logic. The author's "pragmatic" and applied style gives a unique and helpful "non-idealist, practical, opinionate" introduction to digital systems.

Verilog is a Hardware Description Language (HDL) used to design and document electronic systems. Verilog HDL allows designers to virtually design systems without expending time or resources on physical models. It is the most widely used HDL with a user community of more than 50,000 active designers.

VHDL: A Logic Synthesis Approach

VHDL Coding and Logic Synthesis with Synopsys

Introduction to Logic Programming

Coding and RTL Synthesis

From Fundamentals to Quantum Computing

VHDL for Logic Synthesis Second Edition Andrew Rushton TransEDA Limited, Southampton, UK Very high-speed integrated circuit Hardware Description Language (VHDL) is the worldwide standard for computer-aided electronic system design. Logic synthesis automates gate-level design, allowing the designer to concentrate on a rgister-transfer level implementation. VHDL for Logic Synthesis provides comprehensive coverage of the language and its role in the generation of hardware. This enhanced second edition takes a broader view of the use of synthesis and its place in the design cycle. Features include: * Explanation of each aspect of the language in hardware terms and demonstration of the mapping from VHDL to hardware * Updated examples using the standard packages numeric_std and std_logic_1164 plus more illustrative models offering further source references for designers * Additional chapter on std_logic_arith to aid designers still working with this popular package * New focus on libraries and library management covering the contents of the standard library, how to use library work and recommendations on code management * Extra section detailing how to use assertions to report diagnostics, allowing the reader to print signal and variable values to the screen Senior undergraduate and postgraduate students of microelectronics and digital hardware engineers new to language-based design methods will appreciate Rushton's informative introduction to VHDL and its use in logic synthesis.

With an abundance of insightful examples, problems, and computer experiments, Introduction to Logic Design provides a balanced, easy-to-read treatment of the fundamental theory of logic functions and applications to the design of digital devices and systems. Requiring no prior knowledge of electrical circuits or electronics, it supplies the

This textbook for courses in Digital Systems Design introduces students to the fundamental hardware used in modern computers. Coverage includes both the classical approach to digital system design (i.e., pen and paper) in addition to the modern hardware description language (HDL) design approach (computer-based). Using this textbook enables readers to design digital systems using the modern HDL approach, but they have a broad foundation of knowledge of the underlying hardware and theory of their designs. This book is designed to match the way the material is actually taught in the classroom. Topics are presented in a manner which builds foundational knowledge before moving onto advanced topics. The author has designed the presentation with learning goals and assessment at its core. Each section addresses a specific learning outcome that the student should be able to “do” after its completion. The concept checks and exercise problems provide a rich set of assessment tools to measure student performance on each outcome.

Logic Programming is a style of programming in which programs take the form of sets of sentences in the language of Symbolic Logic. Over the years, there has been growing interest in Logic Programming due to applications in deductive databases, automated worksheets, Enterprise Management (business rules), Computational Law, and General Game Playing. This book introduces Logic Programming theory, current technology, and popular applications. In this volume, we take an innovative, model-theoretic approach to logic programming. We begin with the fundamental notion of datasets, i.e., sets of ground atoms. Given this fundamental notion, we introduce views, i.e., virtual relations; and we define classical logic programs as sets of view definitions, written using traditional Prolog-like notation but with semantics given in terms of datasets rather than implementation. We then introduce actions, i.e., additions and deletions of ground atoms; and we define dynamic logic programs as sets of action definitions. In addition to the printed book, there is an online version of the text with an interpreter and a compiler for the language used in the text and an integrated development environment for use in developing and deploying practical logic programs. "This is a book for the 21st century: presenting an elegant and innovative perspective on logic programming. Unlike other texts, it takes datasets as a fundamental notion, thereby bridging the gap between programming languages and knowledge representation languages; and it treats updates on an equal footing with datasets, leading to a sound and practical treatment of action and change." - Bob Kowalski, Professor Emeritus, Imperial College London "In a world where Deep Learning and Python are the talk of the day, this book is a remarkable development. It introduces the reader to the fundamentals of traditional Logic Programming and makes clear the benefits of using the technology to create runnable specifications for complex systems." - Son Cao Tran, Professor in Computer Science, New Mexico State University "Excellent introduction to the fundamentals of Logic Programming. The book is well-written and well-structured. Concepts are explained clearly and the gradually increasing complexity of exercises makes it so that one can understand easy notions quickly before moving on to more difficult ideas." - George Younger, student, Stanford University

Sequential Logic Synthesis

Introduction to Logic Synthesis Using Verilog HDL

Logic Synthesis for Field-Programmable Gate Arrays

Reversible Logic Synthesis

Logic Minimization Algorithms for VLSI Synthesis

Logic synthesis has become a fundamental component of the ASIC design flow, and Logic Synthesis Using Synopsys® has been written for all those who dislike reading manuals but who still like to learn logic synthesis as practised in the real world. The primary focus of the book is Synopsys Design Compiler®: the leading synthesis tool in the EDA marketplace. The book is specially organized to assist designers accustomed to schematic capture based design to develop the required expertise to effectively use the Compiler. Over 100 `classic scenarios' faced by designers using the Design Compiler have been captured and discussed, and solutions provided. The scenarios are based both on personal experiences and actual user queries. A general understanding of the problem-solving techniques provided will help the reader debug similar and more complicated problems. Furthermore, several examples and dc-shell scripts are provided. Specifically, Logic Synthesis Using Synopsys® will help the reader develop a better understanding of the synthesis design flow, optimization strategies using the Design Compiler, test insertion using the Test Compiler®, commonly used interface formats such as EDIF and SDF, and design re-use in a synthesis-based design methodology. Examples have been provided in both VHDL and Verilog. Audience: Written with CAD engineers in mind to enable them to formulate an effective synthesis-based ASIC design methodology. Will also assist design teams to better incorporate and effectively integrate synthesis with their existing in-house design methodology and CAD tools.

This book is structured in a practical, example-driven, manner. The use of VHDL for constructing logic synthesisers is one of the aims of the book; the second is the application of the tools to the design process. Worked examples, questions and answers are provided together with do and don'ts of good practice. An appendix on logic design the source code are available free of charge over the Internet.

This textbook for courses in Digital Systems Design introduces students to the fundamental hardware used in modern computers. Coverage includes both the classical approach to digital system design (i.e., pen and paper) in addition to the modern hardware description language (HDL) design approach (computer-based). Using this textbook enables readers to design digital systems using the modern HDL approach, but they have a broad foundation of knowledge of the underlying hardware and theory of their designs. This book is designed to match the way the material is actually taught in the classroom. Topics are presented in a manner which builds foundational knowledge before moving onto advanced topics. The author has designed the presentation with learning Goals and assessment at its core. Each section addresses a specific learning outcome that the student should be able to “do” after its completion. The concept checks and exercise problems provide a rich set of assessment tools to measure student performance on each outcome.

This book introduces new logic primitives for electronic design automation tools. The author approaches fundamental EDA problems from a different, unconventional perspective, in order to demonstrate the key role of rethinking EDA solutions in overcoming technological limitations of present and future technologies. The author discusses techniques that improve the efficiency of logic representation, manipulation and optimization tasks by taking advantage of majority and biconditional logic primitives. Readers will be enabled to accelerate formal methods by studying core properties of logic circuits and developing new frameworks for logic reasoning engines.

A Guide to Digital Design and Synthesis

Finite State Machine Datapath Design, Optimization, and Implementation

Introduction to Logic Design

Digital Circuits and Systems

Verilog HDL

This book is designed to serve as a hands-on professional reference with additional utility as a textbook for upper undergraduate and some graduate courses in digital logic design. This book is organized in such a way that that it can describe a number of RTL design scenarios, from simple to complex. The book constructs the logic design story from the fundamentals of logic design to advanced RTL design concepts. Keeping in view the importance of miniaturization today, the book gives practical information on the issues with ASIC RTL design and how to overcome these concerns. It clearly explains how to write an efficient RTL code and how to improve design performance. The book also describes advanced RTL design concepts such as low-power design, multiple clock-domain design, and SOC-based design. The practical orientation of the book makes it ideal for training programs for practicing design engineers and for short-term vocational programs. The contents of the book will also make it a useful read for students and hobbyists.

DIGITAL LOGIC

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Switching Theory for Logic Synthesis covers the basic topics of switching theory and logic synthesis in fourteen chapters. Chapters 1 through 5 provide the mathematical foundation. Chapters 6 through 8 include an introduction to sequential circuits, optimization of sequential machines and asynchronous sequential circuits. Chapters 9 through 14 are the main feature of the book. These chapters introduce and explain various topics that make up the subject of logic synthesis: multi-valued input two-valued output function, logic design for PLDs/FPGAs, EXOR-based design, and complexity theories of logic networks. An appendix providing a history of switching theory is included. The reference list consists of over four hundred entries. Switching Theory for Logic Synthesis is based on the author's lectures at Kyushu Institute of Technology as well as seminars for CAD engineers from various Japanese technology companies. Switching Theory for Logic Synthesis will be of interest to CAD professionals and students at the advanced level. It is also useful as a textbook, as each chapter contains examples, illustrations, and exercises.

Pragmatic Logic: Synthesis Lecture On Digital Circuits And Systems

Analysis and Synthesis

Logic Synthesis and Verification

This book covers recent advances in the field of logic synthesis and design, including Boolean Matching, Logic Decomposition, Boolean satisfiability, Advanced Synthesis Techniques and Applications of Logic Design. All of these topics are valuable to CAD engineers working in Logic Design, Logic Optimization, and Verification. Engineers seeking opportunities for optimizing VLSI integrated circuits will find book as an invaluable reference, since there is no existing book that covers this material in a systematic fashion.

Logic Synthesis and Optimization presents up-to-date research information in a pedagogical form. The authors are recognized as the leading experts on the subject. The focus of the book is on logic minimization and includes such topics as two-level minimization, multi-level minimization, application of binary decision diagrams, delay optimization, asynchronous circuits, spectral method for logic design, fielc programmable gate array (FPGA) design, EXOR logic synthesis and technology mapping. Examples and illustrations are included so that each contribution can be read independently. Logic Synthesis and Optimization is an indispensable reference for academic researchers as well as professional CAD engineers.

An Introduction to Logic Circuit Testing provides a detailed coverage of techniques for test generation and testable design of digital electronic circuits/systems. The material covered in the book should be sufficient for a course, or part of a course, in digital circuit testing for senior-level undergraduate and first-year graduate students in Electrical Engineering and Computer Science. The book will also be a valuable resource for engineers working in the industry. This book has four chapters. Chapter 1 deals with various types of faults that may occur in very large scale integration (VLSI)-based digital circuits. Chapter 2 introduces the major concepts of all test generation techniques such as redundancy, fault coverage, sensitization, and backtracking. Chapter 3 introduces the key concepts of testability, followed some ad hoc design-for-testability rules that can be used to enhance testability of combinational circuits. Chapter 4 deals with test generation and response evaluation techniques used in BIST (built-in self-test) schemes for VLSI chips. Table of Contents: Introduction / Fault Detection in Logic Circuits / Design for Testability / Built-in Self-Test / References

Logic Synthesis and Verification Algorithms is a textbook designed for courses on VLSI Logic Synthesis and Verification, Design Automation, CAD and advanced level discrete mathematics. It also serves as a basic reference work in design automation for both professionals and students. Logic Synthesis and Verification Algorithms is about the theoretical underpinnings of VLSI (Very Large Scale Integrated Circuits). It combines and integrates modern developments in logic synthesis and formal verification with the more traditional matter of Switching and Finite Automata Theory. The book also provides background material on Boolean algebra and discrete mathematics. A unique feature of this text is the large collection of solved problems. Throughout the text the algorithms covered are the subject of one or m problems based on the use of available synthesis programs.