Practical Problems In Vlsi Physical Design

This volume is based on the research papers presented in the 4th Computer Science On-line Conference. The volume Artificial Intelligence Perspectives and Applications presents new approaches and methods to real-world problems, and in particular, exploratory research that describes novel approaches in the field of artificial intelligence. Particular emphasis is laid on modern trends in selected fields of interest. New algorithms or methods in a variety of fields are also presented. The Computer Science On-line Conference (CSOC 2015) is intended to provide an international forum for discussions on the latest high-quality research results in all areas related to Computer Science. The addressed topics are the theoretical aspects and applications of Computer Science, Artificial Intelligences, Cybernetics, Automation Control Theory and Software Engineering.

Algorithms for VLSI Physical Design Automation is a core reference text for graduate students and CAD professionals. It provides a comprehensive treatment of the principles and algorithms of VLSI physical design. Algorithms for VLSI Physical Design Automation presents the concepts and algorithms in an intuitive manner. Each chapter contains 3-4 algorithms that are discussed in detail. Additional algorithms are presented in a somewhat shorter format. References to advanced algorithms are presented at the end of each chapter. Algorithms for VLSI Physical Design Automation covers all aspects of physical design. The first three chapters provide the background material while the subsequent chapters focus on each phase of the physical design cycle. In addition, newer topics like physical design automation of FPGAs and MCMs have been included. The author provides an extensive bibliography which is useful for finding advanced material on a topic. Algorithms for VLSI Physical Design Automation is an invaluable reference for professionals in layout, design automation and physical design.

With vastly increased complexity and functionality in the "nanometer era" (i.e. hundreds of millions of transistors on one chip), increasing the performance of integrated circuits has become a challenging task. Connecting effectively (interconnect design) all of these chip elements has become the greatest determining factor in overall performance. 3-D integrated circuit design may offer the best solutions in the near future. This is the first book on 3-D integrated circuit design, covering all of the technological and design aspects of this emerging design paradigm, while proposing effective solutions to specific challenging problems concerning the design of 3-D integrated circuits. A handy, comprehensive reference or a practical design guide, this book provides a sound foundation for the design of 3-D integrated circuits. * Demonstrates how to overcome "interconnect bottleneck" with 3-D integrated circuit design...leading edge design techniques offer solutions to problems (performance/power consumption/price) faced by all circuit designers * The FIRST book on 3-D integrated circuit design...provides up-to-date information that is otherwise difficult to find * Focuses on design issues key to the product development cycle...good design plays a major role in exploiting the implementation flexibilities offered in the 3-D * Provides broad coverage of 3-D integrated circuit design, including interconnect prediction models, thermal management techniques, and timing optimization...offers practical view of designing 3-D circuits

This book addresses two main problems with interconnections at the chip and package level: crosstalk and simultaneous switching noise. Its orientation is towards giving general information rather than a compilation of practical cases. Each chapter contains a list of references for the topics.

Advanced Logic Synthesis

Electronic Design Automation

VLSI Physical Design Automation

Proceedings of the 4th Computer Science On-line Conference 2015 (CSOC2015), Vol 1: Artificial Intelligence Perspectives and Applications

ALGORITHMS VLSI DESIGN AUTOMATION

VLSI is an important area of electronic and computer engineering. However, there are few textbooks available for undergraduate/postgraduate study of VLSI design automation and chip layout. VLSI Physical Design Automation: Theory and Practice fills the void and is an essential introduction for senior undergraduates, postgraduates and anyone starting work in the field of CAD for VLSI. It covers all aspects of physical design, together with such related areas as automatic cell generation, silicon compilation, layout editors and compaction. A problem-solving approach is adopted and each solution is illustrated with examples. Each topic is treated in a standard format: Problem Definition, Cost Functions and Constraints, Possible Approaches and Latest Developments. Special features: The book deals with all aspects of VLSI physical design, from partitioning and floorplanning to layout generation and silicon compilation; provides a comprehensive treatment of most of the popular algorithms; covers the latest developments and gives a bibliography for further research; offers numerous fully described examples, problems and programming exercises.

Based on the authors' expansive collection of notes taken over the years, Nano-CMOS Circuit and Physical Design bridges the gap between physical and circuit design and fabrication processing, manufacturability, and yield. This innovative book covers: process technology, including sub-wavelength optical lithography; impact of process scaling on circuit and physical implementation and low power with leaky transistors; and DFM, yield, and the impact of physical implementation.

Handbook of Approximation Algorithms and Metaheuristics, Second Edition reflects the tremendous growth in the field, over the past two decades. Through contributions from leading experts, this handbook provides a comprehensive introduction to the underlying theory and methodologies, as well as the various applications of approximation algorithms and metaheuristics. Volume 1 of this two-volume set deals primarily with methodologies and traditional applications. It includes restriction, relaxation, local ratio, approximation schemes, randomization, tabu search, evolutionary computation, local search, neural networks, and other metaheuristics. It also explores multi-objective optimization, reoptimization, sensitivity analysis, and stability. Traditional applications covered include: bin packing, multi-dimensional packing, Steiner trees, traveling salesperson, scheduling, and related problems. Volume 2 focuses on the contemporary and emerging applications of methodologies to problems in combinatorial optimization, computational geometry and graphs problems, as well as in large-scale and emerging application areas. It includes approximation algorithms and heuristics for clustering, networks (sensor and wireless), communication, bioinformatics search, streams, virtual communities, and more. About the Editor Teofilo F. Gonzalez is a professor emeritus of computer science at the University of California, Santa Barbara. He completed his Ph.D. in 1975 from the University of Minnesota. He taught at the University of Oklahoma, the Pennsylvania State University, and the University of Texas at Dallas, before joining the UCSB computer science faculty in 1984. He spent sabbatical leaves at the Monterrey Institute of Technology and Higher Education and Utrecht University. He is known for his highly cited pioneering research in the hardness of approximation; for his sublinear and best possible approximation algorithm for k-tMM clustering; for introducing the open-shop scheduling problem as well as algorithms for its solution that have found applications in numerous research areas; as well as for his research on problems in the areas of job scheduling, graph algorithms, computational geometry, message communication, wire routing, etc.

This overview of the security problems in modern VLSI design provides a detailed treatment of a newly developed constraint-based protection paradigm for the protection of VLSI design IPs from FPGA design to standard-cell placement, and from advanced CAD tools to physical design algorithms.

Three-dimensional Integrated Circuit Design

Formal Verification

IP Cores Design from Specifications to Production

Genetic Algorithms: For Vlsi Design, Layout & Test Automation

A Conceptual Taxonomy

Algorithms for VLSI Physical Design Automation

Genetic Algorithms mimic the natural process of evolution, helping engineers optimize their designs by using the principle of "survival of the fittest". VLSI is especially suited to benefit from genetic algorithms- and this comprehensive book shows how to get the best results. You will discover how genetic algorithms work and how you can use them in a wide variety of VLSI design, layout and test automation tasks.

This book presents new methods and approaches to real-world problems as well as exploratory research that describes novel artificial intelligence applications, including deep learning, neural networks and hybrid algorithms. This book constitutes the refereed proceedings of the Artificial Intelligence Trends in Intelligent Systems Section of the 6th Computer Science On-line Conference 2017 (CSOC 2017), held in April 2017.

This book provides a comprehensive overview of the VLSI design process. It covers end-to-end system on chip (SoC) design, including design methodology, the design environment, tools, choice of design components, handoff procedures, and design infrastructure needs. The book also offers critical guidance on the latest UPF-based low power design flow issues for deep submicron SOC designs, which will prepare readers for the challenges of working at the nanotechnology scale. This practical guide will provide engineers who aspire to be VLSI designers with the techniques and tools of the trade, and will also be a valuable professional reference for those already working in VLSI design and verification with a focus on complex SoC designs. A comprehensive practical guide for VLSI designers; Covers end-to-end VLSI SoC design flow; Includes source code, case studies, and application examples.

Practical Problems in VLSI Physical Design Automation contains problems and solutions related to various well-known algorithms used in VLSI physical design automation. Dr. Lim believes that the best way to learn new algorithms is to walk through a small example by hand. This knowledge will greatly help understand, analyze, and improve some of the well-known algorithms. The author has designed and taught a graduate-level course on physical CAD for VLSI at Georgia Tech. Over the years he has written his homework with such a focus and has maintained typeset version of the solutions.

Handbook of Approximation Algorithms and Metaheuristics

Practical Problems in VLSI Physical Design Automation

Modeling, Verification, Optimization, and Protection

Artificial Intelligence Trends in Intelligent Systems

An ASIC Design Implementation Perspective

Routing in the Third Dimension

An important resource for students, engineers and researchers working in the area of thin film deposition using physical vapor deposition (e.g. sputtering) for semiconductor, liquid crystal displays, high density recording media and photovoltaic device (e.g. thin film solar cell) manufacturing. This book also reviews microelectronics industry topics such as history of inventions and technology trends, recent developments in sputtering technologies, manufacturing steps that require sputtering of thin films, the properties of thin films and the role of sputtering target performance on overall productivity of various processes. Two unique chapters of this book deal with productivity and troubleshooting issues. The content of the book has been divided into two sections: (a) the first section (Chapter 1 to Chapter 3) has been prepared for the readers from a range of disciplines (e.g. electrical, chemical, chemistry, physics) trying to get an insight into use of sputtered films in various devices (e.g. semiconductor, display, photovoltaic, data storage), basic of sputtering and performance of sputtering target in relation to productivity, and (b) the second section (Chapter 4 to Chapter 8) has been prepared for readers who already have background knowledge of sputter deposition of thin films, materials science principles and interested in the details of sputtering target manufacturing methods, sputtering behavior and thin film properties specific to semiconductor, liquid crystal display, photovoltaic and magnetic data storage applications. In Chapters 5 to 8, a general structure has been used, i.e. a description of the applications of sputtered thin films, sputtering target manufacturing methods (including flow charts), sputtering behavior of targets (e.g. current - voltage relationship, deposition rate) and thin film properties (e.g. microstructure, stresses, electrical properties, in-film particles). While discussing these topics, attempts have been made to include examples from the actual commercial processes to highlight the increased complexity of the commercial processes with the growth of advanced technologies. In addition to personnel working in industry setting, university researchers with advanced knowledge of sputtering would also find discussion of such topics (e.g. attributes of target design, chamber design, target microstructure, sputter surface characteristics, various troubleshooting issues) useful. . Unique coverage of sputtering target manufacturing methods in the light of semiconductor, displays, data storage and photovoltaic industry requirements Practical information on technology trends, role of sputtering and major OEMs Discussion on properties of a wide variety of thin films which include silicides, conductors, diffusion barriers, transparent conducting oxides, magnetic films etc. Practical case-studies on target performance and troubleshooting Essential technological information for students, engineers and scientists working in the semiconductor, display, data storage and photovoltaic industry

VLSI Design Environments investigates design alternatives such as object oriented data modelling. The difficulty of automating chip architecture designs is caused by the complexity of the problem. The explosion of design decions make a heuristic approach necessary. PLAYOUT aims at the solution of system problems based on hierarchy, top-down plannin

One of the main problems in chip design is the enormous number of possible combinations of individual chip elements within a system, and the problem of their compatibility. The recent application of data structures, efficient algorithms, and ordered binary decision diagrams (OBDDs) has proven vital in designing the computer chips of tomorrow. This book provides an introduction to the foundations of this interdisciplinary research area, emphasizing its applications in computer aided circuit design.

iming, timing, timing! That is the main concern of a digital designer charged with designing a semiconductor chip. What is it, how is it T described, and how does one verify it? The design team of a large digital design may spend months architecting and iterating the design to achieve the required timing target. Besides functional verification, the t- ing closure is the major milestone which dictates when a chip can be - leased to the semiconductor foundry for fabrication. This book addresses the timing verification using static timing analysis for nanometer designs. The book has originated from many years of our working in the area of timing verification for complex nanometer designs. We have come across many design engineers trying to learn the background and various aspects of static timing analysis. Unfortunately, there is no book currently ava- able that can be used by a working engineer to get acquainted with the - tails of static timing analysis. The chip designers lack a central reference for information on timing, that covers the basics to the advanced timing veri- cation procedures and techniques.

Methologies and Traditional Applications, Volume 1

Top-Down Digital VLSI Design

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On Optimal Interconnections for VLSI

Theory and Practice

Proceedings of the 6th Computer Science On-line Conference 2017 (CSOC2017), Vol 1

&Quot;VLSI Physical Design Automation: Theory and Practice is an essential introduction for senior undergraduates, postgraduates and anyone starting work in the field of CAD for VLSI. It covers all aspects of physical design, together with such related areas as automatic cell generation, silicon compilation, layout editors and compaction. A problem-solving approach is adopted and each solution is illustrated with examples. Each topic is treated in a standard format: Problem Definition, Cost Functions and Constraints, Possible Approaches and Latest Developments."--BOOK JACKET.

The physical design flow of any project depends upon the size of the design, the technology, the number of designers, the clock frequency, and the time to do the design. As technology advances and design-styles change, physical design flows are constantly reinvented as traditional phases are removed and new ones are added to accommodate changes in technology. Handbook of Algorithms for Physical Design Automation provides a detailed overview of VLSI physical design automation, emphasizing state-of-the-art techniques, trends and improvements that have emerged during the previous decade. After a brief introduction to the modern physical design problem, basic algorithmic techniques, and partitioning, the book discusses significant advances in floorplanning representations and describes recent formulations of the floorplanning problem. The text also addresses issues of placement, net layout and optimization, routing multiple signal nets, manufacturability, physical synthesis, special nets, and designing for specialized technologies. It includes a personal perspective from Ralph Otten as he looks back on the major technical milestones in the history of physical design automation. Although several books on this topic are currently available, most are either too broad or out of date. Alternatively, proceedings and journal articles are valuable resources for researchers in this area, but the material is widely dispersed in the literature. This handbook pulls together a broad variety of perspectives on the most challenging problems in the field, and focuses on emerging problems and research results.

This book provides broad and comprehensive coverage of the entire EDA flow. EDA/VLSI practitioners and researchers in need of fluency in an "adjacent" field will find this an invaluable reference to the basic EDA concepts, principles, data structures, algorithms, and architectures for the design, verification, and test of VLSI circuits. Anyone who needs to learn the concepts, principles, data structures, algorithms, and architectures of the EDA flow will benefit from this book. Covers complete spectrum of the EDA flow, from ESL design modeling to logic/test synthesis, verification, physical design, and test - helps EDA newcomers to get "up-and-running" quickly Includes comprehensive coverage of EDA concepts, principles, data structures, algorithms, and architectures - helps all readers improve their VLSI design competence Contains latest advancements not yet available in other books, including Test compression, ESL design modeling, large-scale floorplanning, placement, routing, synthesis of clock and power/ground networks - helps readers to design/develop testable chips or products Includes industry best-practices wherever appropriate in most chapters - helps readers avoid costly mistakes

Algorithms for VLSI Physical Design Automation, Third Edition covers all aspects of physical design. The book is a core reference for graduate students and CAD professionals. For students, concepts and algorithms are presented in an intuitive manner. For CAD professionals, the material presents a balance of theory and practice. An extensive bibliography is provided which is useful for finding advanced material on a topic. At the end of each chapter, exercises are provided, which range in complexity from simple to research level. Algorithms for VLSI Physical Design Automation, Third Edition provides a comprehensive background in the principles and algorithms of VLSI physical design. The goal of this book is to serve as a basis for the development of introductory-level graduate courses in VLSI physical design automation. It provides self-contained material for teaching and learning algorithms of physical design. All algorithms which are considered basic have been included, and are presented in an intuitive manner. Yet, at the same time, enough detail is provided so that readers can actually implement the algorithms given in the text and use them. The first three chapters provide the background material, while the focus of each chapter of the rest of the book is on each phase of the physical design cycle. In addition, newer topics such as physical design automation of FPGAs and

MCMs have been included. The basic purpose of the third edition is to investigate the new challenges presented by interconnect and process innovations. In 1995 when the second edition of this book was prepared, a six-layer process and 15 million transistor microprocessors were in advanced stages of design. In 1998, six metal process and 20 million transistor designs are in production. Two new chapters have been added and new material has been included in almost allother chapters. A new chapter on process innovation and its impact on physical design has been added. Another focus of the third edition is to promote use of the Internet as a resource, so wherever possible URLs have been provided for further investigation. Algorithms for VLSI Physical Design Automation, Third Edition is an important core reference work for professionals as well as an advanced level textbook for students.

Practical Low Power Digital VLSI Design

A Practical Approach to VLSI System on Chip (SoC) Design

VLSI Circuit Design Methodology Demystified

Digital Integrated Circuit Design

A Practical Guide

Intellectual Property Protection in VLSI Designs

Market_Desc: · Electrical Engineering Students taking courses on VLSI systems, CAD tools for VLSI, Design Automation at Final Year or Graduate Level, Computer Science courses on the same topics, at a similar level· Practicing Engineers wishing to learn the state of the art in VLSI Design Automation· Designers of CAD tools for chip design in software houses or large electronics companies. Special Features: · Probably the first book on Design Automation for VLSI Systems which covers all stages of design from layout synthesis through logic synthesis to high-level synthesis· Clear, precise presentation of examples, well illustrated with over 200 figures· Focus on algorithms for VLSI design tools means it will appeal to some Computer Science as well as Electrical Engineering departments About The Book: Enrollments in VLSI design automation courses are not large but it's a very popular elective, especially for those seeking a career in the microelectronics industry. Already the reviewers seem very enthusiastic about the coverage of the book being a better match for their courses than available competitors, because it covers all design phases. It has plenty of worked problems and a large no. of illustrations. It's a good 'list-builder' title that matches our strategy of focusing on topics that lie on the interface between Elec Eng and Computer Science.

Since register transfer level (RTL) design is less about being a bright engineer, and more about knowing the downstream implications of your work, this book explains the impact of design decisions taken that may give rise later in the product lifecycle to issues related to testability, data synchronization across clock domains, synthesizability, power consumption, routability, etc., all which are a function of the way the RTL was originally written. Readers will benefit from a highly practical approach to the fundamentals of these topics, and will be given clear guidance regarding necessary safeguards to observe during RTL design.

Very Large Scale Integration (VLSI) has become a necessity rather than a specialization for electrical and computer engineers. This unique text provides Engineering and Computer Science students with a comprehensive study of the subject, covering VLSI from basic design techniques to working principles of physical design automation tools to leading edge application-specific array processors. Beginning with CMOS design, the author describes VLSI design from the viewpoint of a digital circuit engineer. He develops physical pictures for CMOS circuits and demonstrates the top-down design methodology using two design projects - a microprocessor and a field programmable gate array. The author then discusses VLSI testing and dedicates an entire chapter to the working principles, strengths, and weaknesses of ubiquitous physical design tools. Finally, he unveils the frontiers of VLSI. He emphasizes its use as a tool to develop innovative algorithms and architecture to solve previously intractable problems. VLSI Design answers not only the question of "what is VLSI," but also shows how to use VLSI. It provides graduate and upper level undergraduate students with a complete and congregated view of VLSI engineering.

On Optimal Interconnections for VLSI describes, from a geometric perspective, algorithms for high-performance, high-density interconnections during the global and detailed routing phases of circuit layout. First, the book addresses area minimization, with a focus on near-optimal approximation algorithms for minimum-cost Steiner routing. In addition to practical implementations of recent methods, the implications of recent results on spanning tree degree bounds and the method of Zelikovsky are discussed. Second, the book addresses delay minimization, starting with a discussion of accurate, yet algorithmically tractable, delay models. Recent minimum-delay constructions are highlighted, including provably good cost-radius tradeoffs, critical-sink routing algorithms, Elmore delay-optimal routing, graph Steiner arborescences, non-tree routing, and wiresizing. Third, the book addresses skew minimization for clock routing and prescribed-delay routing formulations. The discussion starts with early matching-based constructions and goes on to treat zero-skew routing with provably minimum wirelength, as well as planar clock routing. Finally, the book concludes with a discussion of multiple (competing) objectives, i.e., how to optimize area, delay, skew, and other objectives simultaneously. These techniques are useful when the routing instance has heterogeneous resources or is highly congested, as in FPGA routing, multi-chip packaging, and very dense layouts. Throughout the book, the emphasis is on practical algorithms and a complete self-contained development. On Optimal Interconnections for VLSI will be of use to both circuit designers (CAD tool users) as well as researchers and developers in the area of performance-driven physical design.

A Comprehensive Guide

VLSI Physical Design: From Graph Partitioning to Timing Closure

Parallel Methods for VLSI Layout Design

VLSI Design

From Architectures to Gate-Level Circuits and FPGAs

Nano-CMOS Circuit and Physical Design

Top-Down VLSI Design: From Architectures to Gate-Level Circuits and FPGAs represents a unique approach to learning digital design. Developed from more than 20 years teaching circuit design, Doctor Kaeslin's approach follows the natural VLSI design flow and makes circuit design accessible for professionals with a background in systems engineering or digital signal processing. It begins with hardware architecture and promotes a system-level view, first considering the type of intended application and letting that guide your design choices. Doctor Kaeslin presents modern considerations for handling circuit complexity, throughput, and energy efficiency while preserving functionality. The book focuses on application-specific integrated circuits (ASICs), which along with FPGAs are increasingly used to develop products with applications in telecommunications, IT security, biomedical, automotive, and computer vision industries. Topics include field-programmable logic, algorithms, verification, modeling hardware, synchronous clocking, and more. Demonstrates a top-down approach to digital VLSI design. Provides a systematic overview of architecture optimization techniques. Features a chapter on field-programmable logic devices, their technologies and architectures. Includes checklists, hints, and warnings for various design situations. Emphasizes design flows that do not overlook important action items and which include alternative options when planning the development of microelectronic circuits.

The book provides a comprehensive overview of electromigration and its effects on the reliability of electronic circuits. It introduces the physical process of electromigration, which gives the reader the requisite understanding and knowledge for adopting appropriate counter measures. A comprehensive set of options is presented for modifying the present IC design methodology to prevent electromigration. Finally, the authors show how specific effects can be exploited in present and future technologies to reduce electromigration's negative impact on circuit reliability.

Practical Problems in VLSI Physical Design AutomationSpringer Science & Business Media

- Applicable for bookstore catalogue

Synthesis, Verification, and Test

OBDD - Foundations and Applications

From VLSI Chips to MCMs

VLSI Design Environments

Algorithms and Data Structures in VLSI Design

Physical Design Essentials

Practical Low Power Digital VLSI Design emphasizes the optimization and trade-off techniques that involve power dissipation, in the hope that the readers are better prepared the next time they are presented with a low power design problem. The book highlights the basic principles, methodologies and techniques that are common to most CMOS digital designs. The advantages and disadvantages of a particular low power technique are discussed. Besides the classical area-performance trade-off, the impact to design cycle time, complexity, risk, testability and reusability are discussed. The wide impacts to all aspects of design are what make low power problems challenging and interesting. Heavy emphasis is given to top-down structured design style, with occasional coverage in the semicustom design methodology. The examples and design techniques cited have been known to be applied to production scale designs or laboratory settings. The goal of Practical Low Power Digital VLSI Design is to permit the readers to practice the low power techniques using current generation design style and process technology. Practical Low Power Digital VLSI Design considers a wide range of design abstraction levels spanning circuit, logic, architecture and system. Substantial basic knowledge is provided for qualitative and quantitative analysis at the different design abstraction levels. Low power techniques are presented at the circuit, logic, architecture and system levels. Special techniques that are specific to some key areas of digital chip design are discussed as well as some of the low power techniques that are just appearing on the horizon. Practical Low Power Digital VLSI Design will be of benefit to VLSI design engineers and students who have a fundamental knowledge of CMOS digital design.

This book was written to arm engineers qualified and knowledgeable in the area of VLSI circuits with the essential knowledge they need to get into this exciting field and to help those already in it achieve a higher level of proficiency. Few people truly understand how a large chip is developed, but an understanding of the whole process is necessary to appreciate the importance of each part of it and to understand the process from concept to silicon. It will teach readers how to become better engineers through a practical approach of diagnosing and attacking real-world problems.

Formal Verification: An Essential Toolkit for Modern VLSI Design presents practical approaches for design and validation, with hands-on advice to help working engineers integrate these techniques into their work. Formal Verification (FV) enables a designer to directly analyze and mathematically explore the quality or other aspects of a Register Transfer Level (RTL) design without using simulations. This can reduce time spent validating designs and more quickly reach a final design for manufacturing. Building on a basic knowledge of SystemVerilog, this book demystifies FV and presents the practical applications that are bringing it into mainstream design and validation processes at Intel and other companies. After reading this book, readers will be prepared to introduce FV in their organization and effectively deploy FV techniques to increase design and validation productivity. Learn formal verification algorithms to gain full coverage without exhaustive simulation Understand formal verification tools and how they differ from simulation tools Create instant test benches to gain insight into how models work and find initial bugs Learn from Intel insiders sharing their hard-won knowledge and solutions to complex design problems

Arranged in a format that follows the industry-common ASIC physical design flow, Physical Design Essentials begins with general concepts of an ASIC library, then examines floorplanning, placement, routing, verification, and finally, testing. Among the topics covered are Basic standard cell design, transistor-sizing, and layout styles; Linear, non-linear, and polynomial characterization; Physical design constraints and floorplanning styles; Algorithms used for placement; Clock Tree Synthesis; Parasitic extraction; Electronic Testing, and many more.

A Practical Approach

Particle Swarm Optimization with Applications

From VLSI Architectures to CMOS Fabrication

Interconnection Noise in VLSI Circuits

Artificial Intelligence Perspectives and Applications

Sputtering Materials for VLSI and Thin Film Devices

This key text addresses the complex computer chips of tomorrow which will consist of several layers of metal interconnect, making the interconnect within a chip or a multichip module a three dimensional problem. You'll find an insightful approach to the algorithmic, cell design issues in chip and MCM routing with an emphasis on techniques for eliminating routing area.

Design and optimization of integrated circuits are essential to the creation of new semiconductor chips, and physical optimizations are becoming more prominent as a result of semiconductor scaling. Modern chip design has become so complex that it is largely performed by specialized software, which is frequently updated to address advances in semiconductor technologies and increased problem complexities. A user of such software needs a high-level understanding of the underlying mathematical models and algorithms. On the other hand, a developer of such software must have a keen understanding of computer science aspects, including algorithmic performance bottlenecks and how various algorithms operate and interact. "VLSI Physical Design: From Graph Partitioning to Timing Closure" introduces and compares algorithms that are used during the physical design phase of integrated-circuit design, wherein a geometric chip layout is produced starting from an abstract circuit design. The emphasis is on essential and fundamental techniques, ranging from hypergraph partitioning and circuit placement to timing closure.

This book provides a single-source reference to the state-of-the-art in logic synthesis. Readers will benefit from the authors' expert perspectives on new technologies and logic synthesis, new data structures, big data and logic synthesis, and convergent logic synthesis. The authors describe techniques that will enable readers to take advantage of recent advances in big data techniques and frameworks in order to have better logic synthesis algorithms.

This book describes the life cycle process of IP cores, from specification to production, including IP modeling, verification, optimization, and protection. Various trade-offs in the design process are discussed, including those associated with many of the most common memory cores, controller IPs and system-on-chip (SoC) buses. Readers will also benefit from the author's practical coverage of new verification methodologies. such as bug localization, UVM, and scan-chain. A SoC case study is presented to compare traditional verification with the new verification methodologies. Discusses the entire life cycle process of IP cores, from specification to production, including IP modeling, verification, optimization, and protection; Introduce a deep introduction for Verilog for both implementation and verification point of view. Demonstrates how to use IP in applications such as memory controllers and SoC buses. Describes a new verification methodology called bug localization; Presents a novel scan-chain methodology for RTL debugging; Enables readers to employ UVM methodology in straightforward, practical terms.

Static Timing Analysis for Nanometer Designs

Analog Design for CMOS VLSI Systems

An Essential Toolkit for Modern VLSI Design

Fundamentals of Modern VLSI Devices

Handbook of Algorithms for Physical Design Automation

Principles of VLSI RTL Design

Top-down approach to practical, tool-independent, digital circuit design, reflecting how circuits are designed.

This book is intended to gather recent studies on particle swarm optimization (PSO). In this book, readers can find the recent theoretical developments and applications on PSO algorithm. From the theoretical aspect, PSO has preserved its popularity because of the fast convergence rate, and a lot of hybrid algorithms have recently been developed in order to increase the performance of the algorithm. At the same time, PSO has also been used to solve different kinds of engineering optimization problems. In this book, a reader can find engineering applications of PSO, such as environmental economic dispatch and grid computing.

Learn the basic properties and designs of modern VLSI devices, as well as the factors affecting performance, with this thoroughly updated second edition. The first edition has been widely adopted as a standard textbook in microelectronics in many major US universities and worldwide. The internationally renowned authors highlight the intricate interdependencies and subtle trade-offs between various practically important device parameters, and provide an in-depth discussion of device scaling and scaling limits of CMOS and bipolar devices. Equations and parameters provided are checked continuously against the reality of silicon data, making the book equally useful in practical transistor design and in the classroom. Every chapter has been updated to include the latest developments, such as MOSFET scale length theory, high-field transport model and SiGe-base bipolar devices.

Fundamentals of Electromigration-Aware Integrated Circuit Design