Proceedings International Test Conference 1998

The advent of the digital era, the Internet, and the development of fast com puting devices that can access mass storage servers at high communication bandwidths have brought within our reach the world of ambient intelligent systems. These systems provide users with information, communication, and entertainment at any desired place and time. Since its introduction in 1998, the vision of Ambient Intelligence has attracted much attention within the re search community. Especially, the need for intelligence generated by smart al gorithms, which run on digital platforms that are integrated into consumer elec tronics devices, has strengthened the interest in Computational Intelligence. This newly developing research field, which can be positioned at the inter section of computer science, discrete mathematics, and artificial intelligence, contains a large variety of interesting topics including machine learning, con tent management, vision, speech, data mining, content augmentation, profiling, contextual awareness, feature extraction, resource management, security, and privacy.

Embedded systems are nearly ubiquitous, and books on individual topics or components of embedded systems are equally abundant. Unfortunately, for those designers who thirst for knowledge of the big picture of embedded systems there is not a drop to drink. Until now. The Embedded Systems Handbook is an oasis of information, offering a mix of basic a

System-on-Chip (SoC) represents the next major market for microelectronics, and there is considerable interest world-wide in developing effective methods and tools to support the SoC

paradigm. SoC is an expanding field, at present the technical and technological literature about the overall state-of-the-art in SoC is dispersed across a wide spectrum which includes books, journals, and conference proceedings. The book provides a comprehensive and accessible source of state-of-the-art information on existing and emerging SoC key research areas, provided by leading experts in the field. This book covers the general principles of designing, validating and testing complex embedded computing systems and their underlying tradeoffs. The book has twenty five chapters organised into eight parts, each part focuses on a particular topic of SoC. Each chapter has some background covering the basic principles, and extensive list of references. It is aimed at graduate students, designers and managers working in Electronic and Computer engineering.

The Boundary — Scan Handbook

International Test Conference : 1998

Information and Business Intelligence

Proceedings, International Test Conference 1997

Advanced Test Methods for SRAMs

Microelectronic Test Structures, 1998. ICMTS 1998., Proceedings of the 1998 International Conference on

This book contains extended and revised versions of the best papers presented at the 25th IFIP WG 10.5/IEEE International Conference on Very Large Scale Integration, VLSI-SoC 2017, held in Abu Dhabi, United Arab Emirates, in August 2017. The 11 papers included in this book were carefully reviewed and selected

from the 33 full papers presented at the conference. The papers cover a wide range of topics in VLSI technology and advanced research. They address the latest scientific and industrial results and developments as well as future trends in the field of System-on-Chip (SoC) Design. On the occasion of the silver jubilee of the VLSI-SoC conference series the book also includes a special chapter that presents the history of the VLSI-SoC series of conferences and its relation with VLSI-SoC evolution since the early 80s up to the present.

This book grew out of an attempt to describe a variety of tools that were developed over a period of years in IBM to analyze Integrated Circuit fail data. The selection presented in this book focuses on those tools that have a significant statistical or datamining component. The danger of describing sta tistical analysis methods is the amount of non-trivial mathematics that is involved and that tends to obscure the usually straigthforward analysis ideas. This book is, therefore, divided into two roughly equal parts. The first part contains the description of the various analysis techniques and focuses on ideas and experimental results. The second part contains all the mathematical details that are necessary to prove the validity of the analysis techniques, the existence of solutions to the problems that those techniques engender, and the correctness of several properties that were assumed in the first part. Those who are interested only in using the analysis techniques themselves can skip the second part, but that part is important, if only to understand what is being

done.

The 2nd edition of defect oriented testing has been extensively updated. New chapters on Functional, Parametric Defect Models and Inductive fault Analysis and Yield Engineering have been added to provide a link between defect sources and yield. The chapter on RAM testing has been updated with focus on parametric and SRAM stability testing. Similarly, newer material has been incorporated in digital fault modeling and analog testing chapters. The strength of Defect Oriented Testing for nano-Metric CMOS VLSIs lies in its industrial relevance.

ICMTS 1998

Testing for Small-Delay Defects in Nanoscale CMOS Integrated Circuits

International Conference, IBI 2011, Chongqing, China, December 23-25, 2011. Proceedings, Part I

Algorithms in Ambient Intelligence

Next Generation Electronics

25th IFIP WG 10.5/IEEE International Conference on Very Large Scale Integration, VLSI-SoC 2017, Abu Dhabi, United Arab Emirates, October 23–25, 2017, Revised and Extended Selected Papers

In 2007 The Design, Automation and Test in Europe (DATE) conference celebrated its tenth anniversary. As a tribute to the chip and system-level design and design technology community,

this book presents a compilation of the three most influential papers of each year. This provides an excellent historical overview of the evolution of a domain that contributed substantially to the growth and competitiveness of the circuit electronics and systems industry.

In the early days of digital design, we were concerned with the logical correctness of circuits. We knew that if we slowed down the clock signal sufficiently, the circuit would function correctly. With improvements in the semiconductor process technology, our expectations on speed have soared. A frequently asked question in the last decade has been how fast can the clock run. This puts significant demands on timing analysis and delay testing. Fueled by the above events, a tremendous growth has occurred in the research on delay testing. Recent work includes fault models, algorithms for test generation and fault simulation, and methods for design and synthesis for testability. The authors of this book, Angela Krstic and Tim Cheng, have personally contributed to this research. Now they do an even greater service to the profession by collecting the work of a large number of researchers. In addition to expounding such

a great deal of information, they have delivered it with utmost clarity. To further the reader's understanding many key concepts are illustrated by simple examples. The basic ideas of delay testing have reached a level of maturity that makes them suitable for practice. In that sense, this book is the best x DELAY FAULT TESTING FOR VLSI CIRCUITS available guide for an engineer designing or testing VLSI systems. Tech niques for path delay testing and for use of slower test equipment to test high-speed circuits are of particular interest.

Advances in design methods and process technologies have resulted in a continuous increase in the complexity of integrated circuits (ICs). However, the increased complexity and nanometer-size features of modern ICs make them susceptible to manufacturing defects, as well as performance and quality issues. Testing for Small-Delay Defects in Nanoscale CMOS Integrated Circuits covers common problems in areas such as process variations, power supply noise, crosstalk, resistive opens/bridges, and design-for-manufacturing (DfM)-related rule violations. The book also addresses testing for small-delay defects (SDDs), which can cause immediate timing failures on

both critical and non-critical paths in the circuit. Overviews semiconductor industry test challenges and the need for SDD testing, including basic concepts and introductory material Describes algorithmic solutions incorporated in commercial tools from Mentor Graphics Reviews SDD testing based on "alternative methods" that explores new metrics, top-off ATPG, and circuit topology-based solutions Highlights the advantages and disadvantages of a diverse set of metrics, and identifies scope for improvement Written from the triple viewpoint of university researchers, EDA tool developers, and chip designers and tool users, this book is the first of its kind to address all aspects of SDD testing from such a diverse perspective. The book is designed as a one-stop reference for current industrial practices, research challenges in the domain of SDD testing, and recent developments in SDD solutions.

Defect-Oriented Testing for Nano-Metric CMOS VLSI Circuits

Design of Hardware/Software Embedded Systems

Failure Analysis of Integrated Circuits

Computer Engineering & Apps

VLSI-SoC: Opportunities and Challenges Beyond the Internet of

Things
Modern Techniques

This proceedings volume archives the contributions of the speakers who attended the NATO Advanced Research Workshop on "Science and Technology of Semiconductor-On-Insulator Structures and Devices Operating in a Harsh Environment" held at the Sanatorium Puscha Ozerna, th th Kyiv, Ukraine, from 25 to 29 April 2004. The semiconductor industry has maintained a very rapid growth during the last three decades through impressive technological achievements which have resulted in products with higher performance and lower cost per function. After many years of development semiconductor-on-insulator materials have entered volume production and will increasingly be used by the manufacturing industry. The wider use of semiconductor (especially silicon) on insulator materials will not only enable the benefits of these materials to be further demonstrated but, also, will drive down the cost of substrates which, in turn, will stimulate the development of other novel devices and applications. In itself this trend will encourage the promotion of the skills and ideas generated by researchers in the Former Soviet Union and Eastern Europe and their incorporation in future collaborations.

"This book covers aspects of system design and efficient modelling, and also introduces various fault models and fault mechanisms associated with digital circuits integrated into System on Chip (SoC), Multi-Processor System-on Chip (MPSoC) or Network on Chip (NoC)"--

Kevin Zhang Advancement of semiconductor technology has driven the rapid growth of

very large scale integrated (VLSI) systems for increasingly broad applications, incl- ing high-end and mobile computing, consumer electronics such as 3D gaming, multi-function or smart phone, and various set-top players and ubiquitous sensor and medical devices. To meet the increasing demand for higher performance and lower power consumption in many different system applications, it is often required to have a large amount of on-die or embedded memory to support the need of data bandwidth in a system. The varieties of embedded memory in a given system have alsobecome increasingly more complex, ranging fromstatictodynamic and volatile to nonvolatile. Among embedded memories, six-transistor (6T)-based static random access memory (SRAM) continues to play a pivotal role in nearly all VLSI systems due to its superior speed and full compatibility with logic process technology. But as the technology scaling continues, SRAM design is facing severe challenge in mainta- ing suf?cient cell stability margin under relentless area scaling. Meanwhile, rapid expansion in mobile application, including new emerging application in sensor and medical devices, requires far more aggressive voltage scaling to meet very str- gent power constraint. Many innovative circuit topologies and techniques have been extensively explored in recent years to address these challenges.

Design and Test Technology for Dependable Systems-on-chip

1998 IEEE International Test Conference

ISTFA 2019: Proceedings of the 45th International Symposium for Testing and Failure Analysis

Intl Test Conference 1998 Proceedings

Design for Testability, Debug and Reliability
Design for AT-Speed Test, Diagnosis and Measurement

Modern electronics depend on nanoscaled technologies that present new challenges in terms of testing and diagnostics. Memories are particularly prone to defects since they exploit the technology limits to get the highest density. This book is an invaluable guide to the testing and diagnostics of the latest generation of SRAM, one of the most widely applied types of memory. Classical methods for testing memory are designed to handle the so-called "static faults," but these test solutions are not sufficient for faults that are emerging in the latest Very Deep Sub-Micron (VDSM) technologies. These new fault models, referred to as "dynamic faults", are not covered by classical test solutions and require the dedicated test sequences presented in this book.

In February of 1990, the balloting process for the IEEE proposed standard P1149.1 was completed creating IEEE Std 1149.1-1990. Later that summer, in record time, the standard won ratification as an ANSI standard as well. This completed over six years of intensive cooperative effort by a diverse group of people who share a vision on

solving some of the severe testing problems that exist now and are steadily getting worse. Early in this process, someone asked me if 1 thought that the P1I49.I effort would ever bear fruit. 1 responded somewhat glibly that "it was anyone's guess". Well, it wasn't anyone's guess, but rather the faith of a few individuals in the proposition that many testing problems could be solved if a multifaceted industry could agree on a standard for all to follow. Four of these individuals stand out; they are Harry Bleeker, Colin Maunder, Rodham Tulloss, and Lee Whetsel. In that I am convinced that the 1149.1 standard is the most significant testing development in the last 20 years, I personally feel a debt of gratitude to them and all the people who labored on the various Working Groups in its creation.

Design for AT-Speed Test, Diagnosis and Measurement is the first book to offer practical and proven design-for-testability (DFT) solutions to chip and system design engineers, test engineers and product managers at the silicon level as well as at the board and systems levels. Designers will see how the implementation of embedded test enables simplification of silicon debug and system bring-up. Test engineers will determine how embedded test provides a superior level

of at-speed test, diagnosis and measurement without exceeding the capabilities of their equipment. Product managers will learn how the time, resources and costs associated with test development, manufacture cost and lifecycle maintenance of their products can be significantly reduced by designing embedded test in the product. A complete design flow and analysis of the impact of embedded test on a design makes this book a `must read' before any DFT is attempted.

Design, Automation, and Test in Europe

SOC (System-on-a-Chip) Testing for Plug and Play Test Automation

Accelerating Test, Validation and Debug of High Speed Serial Interfaces

Delay Fault Testing for VLSI Circuits

The Most Influential Papers of 10 Years DATE

Advances in Electronic Testing

Este libro presenta los desafíos planteados por las nuevas y sumamente poderosas tecnologías de integración de sistemas electrónicos, que están en la base de los cambios sociales hacia lo que llaman la Sociedad de la Información; en la que los dispositivos electrónicos se harán una parte incorporada de la vida diaria, encajados en casi cada producto. Es necesario un conocimiento cuidadoso de los desafíos para aprovechar la amplia gama de ocasiones ofrecidas por tales capacidades

de integración y las correspondientes posibilidades de diseño de sistemas electrónicos.

This book first provides a comprehensive coverage of state-of-the-art validation solutions based on real-time signal tracing to guarantee the correctness of VLSI circuits. The authors discuss several key challenges in post-silicon validation and provide automated solutions that are systematic and cost-effective. A series of automatic tracing solutions and innovative design for debug (DfD) techniques are described, including techniques for trace signal selection for enhancing visibility of functional errors, a multiplexed signal tracing strategy for improving functional error detection, a tracing solution for debugging electrical errors, an interconnection fabric for increasing data bandwidth and supporting multi-core debug, an interconnection fabric design and optimization technique to increase transfer flexibility and a DfD design and associated tracing solution for improving debug efficiency and expanding tracing window. The solutions presented in this book improve the validation quality of VLSI circuits, and ultimately enable the design and fabrication of reliable electronic devices.

The theme for the 2019 conference is Novel Computing Architectures. Papers will include discussions on the advent of Artificial Intelligence and the promise of quantum computing that are driving

disruptive computing architectures; Neuromorphic chip designs on one hand, and Quantum Bits on the other, still in R&D, will introduce new computing circuitry and memory elements, novel materials, and different test methodologies. These novel computing architectures will require further innovation which is best achieved through a collaborative Failure Analysis community composed of chip manufacturers, tool vendors, and universities.

Trace-Based Post-Silicon Validation for VLSI Circuits

Proceedings of the NATO Advanced Research Workshop on Science and Technology of Semiconductor-On-Insulator Structures and Devices Operating in a Harsh Environment, Kiev, Ukraine, 26-30 April 2004

1998

Models in Hardware Testing

Lecture Notes of the Forum in Honor of Christian Landrault

System-on-Chip

Embedded Processor-Based Self-Test is a guide to self-testing strategies for embedded processors. Embedded processors are regularly used today in most System-on-Chips (SoCs). Testing of microprocessors and embedded processors has always been a challenge because most traditional testing techniques fail when applied to them. This is due to the complex sequential structure of processor architectures, which consists of high performance datapath units and

sophisticated control logic for performance optimization. Structured Design-for-Testability (DfT) and hardware-based self-testing techniques, which usually have a non-trivial impact on a circuit's performance, size and power, can not be applied without serious consideration and careful incorporation into the processor design. Embedded Processor-Based Self-Test shows how the powerful embedded functionality that processors offer can be utilized as a self-testing resource. Through a discussion of different strategies the book emphasizes on the emerging area of Software-Based Self-Testing (SBST). SBST is based on the idea of execution of embedded software programs to perform self-testing of the processor itself and its surrounding blocks in the SoC. SBST is a low-cost strategy in terms of overhead (area, speed, power), development effort and test application cost, as it is applied using low-cost, low-speed test equipment. Embedded Processor-Based Self-Test can be used by designers, DfT engineers, test practitioners, researchers and students working on digital testing, and in particular processor and SoC test. This book sets the framework for comparisons among different SBST methodologies by discussing key requirements. It presents successful applications of SBST to a number of embedded processors of different complexities and instruction set architectures.

Very Large-Scale Integration (VLSI) creates an integrated circuit (IC) by

combining thousands of transistors into a single chip. While designing a circuit, reduction of power consumption is a great challenge. VLSI designs reduce the size of circuits which eventually reduces the power consumption of the devices. However, it increases the complexity of the digital system. Therefore, computer-aided design tools are introduced into hardware design processes. Unlike the general-purpose computer, an embedded system is engineered to manage a wide range of processing tasks. Single or multiple processing cores manage embedded systems in the form of microcontrollers, digital signal processors, field-programmable gate arrays, and application-specific integrated circuits. Security threats have become a significant issue since most embedded systems lack security even more than personal computers. Many embedded systems hacking tools are readily available on the internet. Hacking in the PDAs and modems is a pervasive example of embedded systems hacking. This book explores the designs of VLSI circuits and embedded systems. These two vast topics are divided into four parts. In the book's first part, the Decision Diagrams (DD) have been covered. DDs have extensively used Computer-Aided Design (CAD) software to synthesize circuits and formal verification. The book's second part mainly covers the design architectures of Multiple-Valued Logic (MVL) Circuits. MVL circuits offer several potential opportunities to improve present VLSI circuit

designs. The book's third part deals with Programmable Logic Devices (PLD). PLDs can be programmed to incorporate a complex logic function within a single IC for VLSI circuits and Embedded Systems. The fourth part of the book concentrates on the design architectures of Complex Digital Circuits of Embedded Systems. As a whole, from this book, core researchers, academicians, and students will get the complete picture of VLSI Circuits and Embedded Systems and their applications.

ProceedingsInternational Test Conference : 1998Proceedings International Test Conference 1998 (IEEE Cat. No.98CH36270).1998 IEEE International Test ConferenceIEEEIntl Test Conference 1998 ProceedingsInstitute of Electrical & Electronics Engineers(IEEE)Proceedings, International Test Conference 1997Proceedings1998The Boundary — Scan HandbookSpringer Science & Business Media

Proceedings

Challenges and Methodologies

Data Mining and Diagnosing IC Fails

Integrated Circuit Test Engineering

Proceedings of the 1998 IEEE International Conference on Microelectronic Test Structures, March 23-26, 1998, Kanazawa, Japan

Embedded Processor-Based Self-Test

Model based testing is the most powerful technique for testing hardware and software systems. Models in Hardware Testing describes the use of models at all the levels of hardware testing. The relevant fault models for nanoscaled CMOS technology are introduced, and their implications on fault simulation, automatic test pattern generation, fault diagnosis, memory testing and power aware testing are discussed. Models and the corresponding algorithms are considered with respect to the most recent state of the art, and they are put into a historical context by a concluding chapter on the use of physical fault models in fault tolerance.

This "must have" reference work for semiconductor professionals and researchers provides a basic understanding of how the most commonly used tools and techniques in silicon-based semiconductors are applied to understanding the root cause of electrical failures in integrated circuits.

Using the book and the software provided with it, the reader can build his/her own tester arrangement to investigate key aspects of analog-, digital- and mixed system circuits Plan of attack based on traditional testing, circuit design and circuit manufacture allows the reader to appreciate a testing regime from the point of view of all the participating interests Worked examples based on theoretical bookwork, practical experimentation and simulation exercises teach the reader how to test circuits thoroughly and effectively

Next Generation Measures Using Formal Techniques

Proceedings International Test Conference 1998 (IEEE Cat. No.98CH36270).

Nature-Inspired VLSI Circuits - From Concept to Implementation
Effective Solutions for Dynamic Fault Detection in Nanoscaled Technologies

Embedded Systems Handbook

This two-volume set (CCIS 267 and CCIS 268) constitutes the refereed proceedings of the International Conference on Information and Business Intelligence, IBI 2011, held in Chongqing, China, in December 2011. The 229 full papers presented were carefully reviewed and selected from 745 submissions. The papers address topics such as communication systems; accounting and agribusiness; information education and educational technology; manufacturing engineering; multimedia convergence; security and trust computing; business teaching and education; international business and marketing; economics and finance; and control systems and digital convergence.

This book introduces several novel approaches to pave the way for the next generation of integrated circuits, which can be successfully and reliably integrated, even in safety-critical applications. The authors describe new measures to address the rising challenges in the field of design for testability, debug, and reliability, as strictly required for state-of-the-art circuit designs. In particular, this book combines formal techniques, such

as the Satisfiability (SAT) problem and the Bounded Model Checking (BMC), to address the arising challenges concerning the increase in test data volume, as well as test application time and the required reliability. All methods are discussed in detail and evaluated extensively, while considering industry-relevant benchmark candidates. All measures have been integrated into a common framework, which implements standardized software/hardware interfaces.

High-Speed Serial Interface (HSSI) devices have become widespread in communications, from the embedded to high-performance computing systems, and from on-chip to a wide haul. Testing of HSSIs has been a challenging topic because of signal integrity issues, long test time and the need of expensive instruments. Accelerating Test, Validation and Debug of High Speed Serial Interfaces provides innovative test and debug approaches and detailed instructions on how to arrive to practical test of modern high-speed interfaces. Accelerating Test, Validation and Debug of High Speed Serial Interfaces first proposes a new algorithm that enables us to perform receiver test more than 1000 times faster. Then an under-sampling based transmitter test scheme is presented. The scheme can accurately extract the transmitter jitter and finish the whole transmitter test within 100ms, while the test usually takes seconds. The book also

presents and external loopback-based testing scheme, where and FPGA-based BER tester and a novel jitter injection technique are proposed. These schemes can be applied to validate, test and debug HSSIs with data rate up to 12.5Gbps at a lower test cost than pure ATE solutions. In addition, the book introduces an efficieng scheme to implement high performance Gaussian noise generators, suitable for evaluating BER performance under noise conditions.

Science and Technology of Semiconductor-On-Insulator Structures and Devices Operating in a Harsh Environment

VLSI Circuits and Embedded Systems

Reliability, Availability and Serviceability of Networks-on-Chip

Embedded Memories for Nano-Scale VLSIs

Tools and Techniques

This is a new type of edited volume in the Frontiers in Electronic Testing book series devoted to recent advances in electronic circuits testing. The book is a comprehensive elaboration on important topics which capture major research and development efforts today. "Hot" topics of current interest to test technology community have been selected, and the authors are key contributors in the corresponding topics.

System-on-a-Chip (SOC) integrated circuits composed of embedded cores

are now commonplace. Nevertheless, there remain several roadblocks to rapid and efficient system integration. Test development is seen as a major bottleneck in SOC design and manufacturing capabilities. Testing SOCs is especially challenging in the absence of standardized test structures, test automation tools, and test protocols. In addition, long interconnects, high density, and high-speed designs lead to new types of faults involving crosstalk and signal integrity. SOC (System-on-a-Chip) Testing for Plug and Play Test Automation is an edited work containing thirteen contributions that address various aspects of SOC testing. SOC (System-on-a-Chip) Testing for Plug and Play Test Automation is a valuable reference for researchers and students interested in various aspects of SOC testing. This book presents an overview of the issues related to the test, diagnosis and fault-tolerance of Network on Chip-based systems. It is the first book dedicated to the quality aspects of NoC-based systems and will serve as an invaluable reference to the problems, challenges, solutions, and trade-offs related to designing and implementing state-of-the-art, on-chip communication architectures.